

DESIGN OF LARGE TIME-CONSTANT SWITCHED-CAPACITOR  
FILTERS FOR BIOMEDICAL APPLICATIONS

A Thesis

by

SANJAY TUMATI

Submitted to the Office of Graduate Studies of  
Texas A&M University  
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2004

Major Subject: Electrical Engineering

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## ABSTRACT

Design of Large Time-Constant Switched-Capacitor Filters

for Biomedical Applications.

(December 2004)

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This thesis investigates the various techniques to achieve large time constants and the ultimate limitations therein. A novel circuit technique for the realization of large time constants for high pass corners in switched-capacitor filters is also proposed and compared with existing techniques. The switched-capacitor technique is insensitive to parasitic capacitances and is area efficient and it requires only two clock phases. The circuit is used to build a typical switched-capacitor front end with a gain of 10. The low pass corner is fixed at 200 Hz. The high pass corner is varied from 0.159Hz to 4 Hz and various performance parameters, such as power consumption, silicon area etc., are compared with conventional techniques and the advantages and disadvantages of each technique are demonstrated. The front-ends are fully differential and are chopper stabilized to protect against DC offsets and  $1/f$  noise. The front-end is implemented in AMI0.6 $\mu$ m technology with a supply voltage of 1.6V and all transistors operate in weak inversion with currents in the range of tens of nano-amperes.

## DEDICATION

To my Late Grandmother

## ACKNOWLEDGEMENTS

I gratefully acknowledge my advisor Dr. Jose Silva-Martinez for giving me great freedom in choosing a thesis topic and then patiently answering my queries and keeping me on the right track. Dr. Silva has this amazing ability to quickly penetrate the core of any circuit which would elude me for weeks. This ability of his used to be a great source of embarrassment to me (and as I later found out, to almost everyone who had technical discussions with him). However, it was possibly the best training I could get in analyzing circuits in an intuitive non-mathematical way. I am also thankful to Dr. Jay R. Porter who has been my employer, an excellent one at that, for almost my entire stay at A&M. I would like to thank David Genzer, Dr. Ashok Nedungadi and Dr. Lee Hudson of Biotronik GmbH for giving me an opportunity to intern with them. They effectively suggested my thesis topic and addressed many practical issues and concerns that I have had. I would like to thank Dr. Cilingiroglu for his excellent course on device physics. Thanks to him, I am no longer afraid of device physics. His friendly manner and his humility in spite of his apparent genius for device physics have made a deep impression on me. Finally, I would like to thank my father for keeping me calm when things threatened to overwhelm me and my mother for constantly calling me and asking me if I was done with my thesis already. Without this kind of outside support, this thesis would never have been completed.

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# CHAPTER I

## INTRODUCTION

### 1.1 Motivation

The realization of large time constants on-chip is of considerable interest in biomedical and electrochemical applications, which require real time processing of analog voltages [1]. One example is a pre-amp used in a pacemaker circuit. Other examples include some biomedical applications in which stand alone differentiators and high pass filters are required [2,3]. In this thesis, we explore the problem of large time constants and present some novel differentiators and high pass structures, which realize large time constants. The novel structures will be used in a biomedical switched-capacitor pre-amplifier, which is used in pacemaker circuits.

In pacemaker circuits, whenever the heart is given a pacing pulse, the heart responds through a set of signals. The response of the heart to a pacing pulse is referred to as the *evoked response*. This response is first captured by the analog front-end, amplified, filtered and fed to the DSP core. The DSP core performs signal processing on this amplified and filtered version of the response and the decision circuit uses the results of this processing. A block level schematic of a pacemaker [4] is given in Fig. 1-1. To make an intelligent decision, the pacemaker front end needs to capture as much information as possible in the *evoked response*.

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This thesis follows the style and format of *IEEE Journal of Solid State Circuits*.

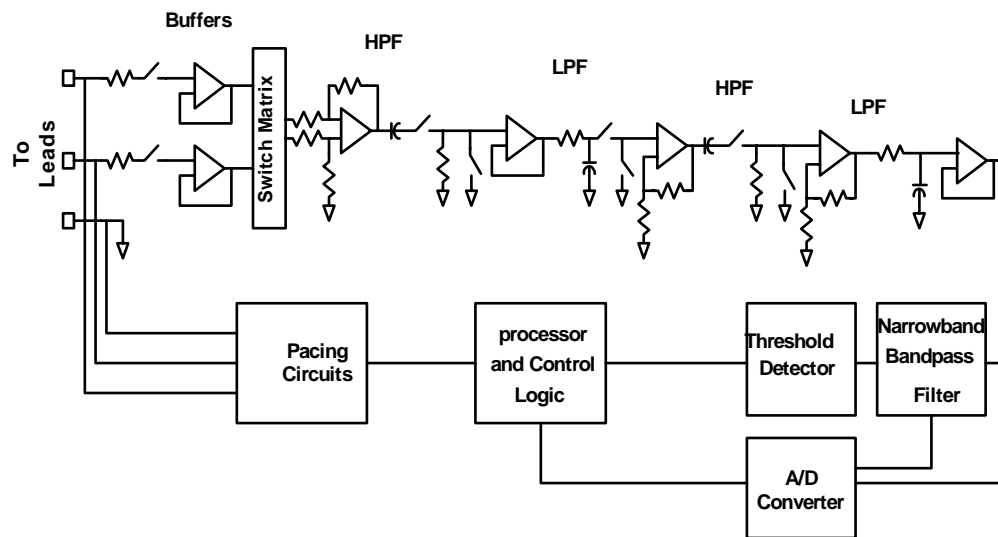


Fig. 1-1: Experimental pacemaker

The front end is basically a filter, which provides amplification to the evoked response. The input to the front end comes from the leads that are connected to the various chambers of the heart (left/right atrium/ventricle). The wideband analog front-End consists of all circuits up to the Narrow-Band Band-pass filter and the ADC.

The front end includes the following:

1. High input impedance buffers so as not to load the heart chambers.
2. A switch matrix to multiplex the inputs from the leads. There are a total of 8 input leads. Only two have been shown in Fig. 1.1.
3. The first HPF, which consists of a differential amplifier providing a gain of 10 and passive RC components.
4. The first LPF, which consists of a buffer and passive RC components.
5. A second HPF incorporating a gain of 5.

6. A second LPF incorporating a gain of 2.
7. A buffer at the end to interface with the narrow band filter and the rest of the digital circuitry.
8. One must have also observed a large number of switches in what appears to be continuous time circuitry. The reason for the switches is that the Front end must be switched on gradually. First the high pass switches on and is given some time to settle down to its steady state. Once the high pass settles, the low pass filter switches ON and so on and so forth. The reason for switching on the front-end gradually is that if a large device with such high open loop gain is switched on all at once, there will be a considerable amount of ringing. And this ringing might bury the evoked response.

It must be mentioned here that Fig. 1-1 is only a conceptual discrete implementation. The actual on-chip implementation will be considerably different as will be discussed later in this chapter.

The *evoked response* contains useful information in frequencies less than 1Hz. The information can be processed by the DSP in the pacemaker to decide on whether a pacing pulse must be given to the heart. More sophisticated pacemakers are expected to decide on even the amplitude and duration of the pacing pulse. Since the pulse generator in the pacing circuit consumes so much power, it is not desirable to give the heart a pacing pulse when it is not needed. Thus the front-end needs to capture the *evoked response* with a fair amount of accuracy, i.e. low distortion, high SNR and accurate filter corners. Currently the biomedical industry uses front-ends with a high pass corner of 4



Hz and a low pass corner of 200 Hz with a clock frequency of 2.5KHz. The main aim is to push the high pass corner to sub-hertz frequencies.

## 1.2 On-chip Implementation

The block diagram in Fig. 1-1 shows the discrete realization of the pacemaker front-end. However, an on-chip realization is required. The problem with on-chip implementations is that precise resistors and capacitors are not available on-chip in most CMOS processes. Typically the RC time-constant varies by 20%. Thus, either Laser trimming is required for on-chip passive components or else they have to go off-chip. Both options are expensive.

Switched-capacitor implementations can offer very accurate time constants and are thus ideal for low frequency applications such as pacemaker circuitry. Another advantage is that switched-capacitor circuits are very linear. Continuous time circuits based on transconductances inherit their non-linearity from the MOS transistor. Switched-capacitor circuits are much less dependent on the non-linearity of the MOS transistor.

However, we cannot completely eliminate the continuous time circuitry. The reason is that switched-capacitor circuits cause aliasing (down-conversion) of high frequency noise to low frequencies and degrade the SNR. Thus a continuous time anti-aliasing low pass filter will always be required to attenuate the high frequency noise before it is aliased by the switched-capacitor circuitry. Fig. 1-2 shows a high level block diagram of an on-chip pacemaker pre-amp.

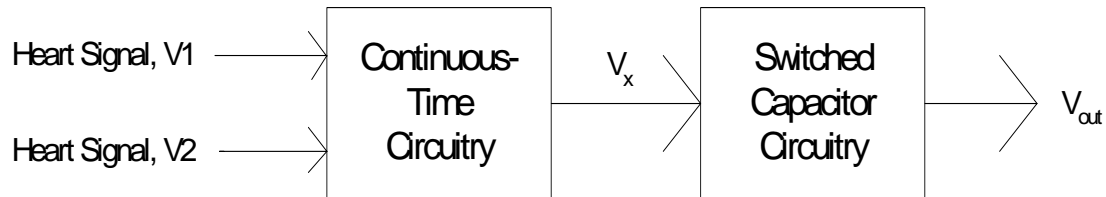


Fig. 1-2: High level block diagram of pacemaker pre-amp

The continuous time circuitry consists of:

1. A low noise gain stage of 10. This ensures that the noise of succeeding stages is less important. This is similar to the use of Low Noise amplifiers in RF front-ends.
2. A high pass filter to remove the offsets, which are residues from the pacing pulse.
3. A low pass anti-aliasing filter.

The switched-capacitor circuitry consists of a high pass filter, a low pass filter and an amplifier with a gain of 10. Thus the complete front end has a second order roll off for both the high pass and low pass corners and a combined gain of 100.

### 1.3 The Switched-Capacitor Circuitry

Our focus here is the switched-capacitor circuitry and the problem of realizing large time constants therein. The switched-capacitor circuitry has a gain of 10, a low pass corner of 4Hz and a high pass corner of 200 Hz. In addition, the continuous time circuitry is followed immediately by a switched-capacitor S/H hold stage to isolate the continuous

time circuitry from the switched-capacitor circuitry. A S/H stage is used as a buffer between the blocks to prevent loading on the continuous circuitry and the switched-capacitor circuitry.

The realization of large time constants is the main bottleneck in the design of the front-end. The clock frequency is 3-4 orders of magnitude larger than the high pass corner. Two factors are involved in the selection of 2.5 KHz as the clock frequency. One is the low pass corner (quite high at 200 Hz) and the other is the need to maintain compatibility with the rest of the system. If conventional switched-capacitor structures are used in the above applications, the capacitor ratios tend to be large enough to discourage their implementation in integrated circuits.

Many techniques have been proposed to implement large time constants [5-9]. These techniques will be discussed in subsequent chapters. All of the techniques are for use in integrators or in first order low pass sections. To the author's knowledge, there is no technique yet to achieve large time constants in first order high pass sections or differentiators. Switched-capacitor differentiators are used in audio codecs and in some biomedical applications [2,3]. It is quite intuitive that the best way to achieve a high pass corner is through the use of high pass sections rather than by combining low pass sections and amplifiers. We will see that this intuition holds in some cases, but not in others.

Conventionally, there are two methods to achieve a high pass corner in switched-capacitor circuits.

1. *Band-pass biquads*: Biquads are usually used in narrow band filtering applications where complex poles are required. In pacemaker applications, the front-end is a wideband filter and hence it is hard to justify using a biquad. One reason is that wideband transfer functions realized using Bi-quads have a greater passband ripple than by using first order sections. The other reason is that in wideband applications, biquads introduce greater errors than first order sections. Biquads, in general, also have lower dynamic range than first order sections. Further, in any implementations of band pass functions using ideal biquads, the zero of the transfer function is at DC. However, in real biquads, due to finite DC gain of the op-amps, the zero of the transfer function is not at DC. Rather, it is at a low frequency. This low frequency zero introduces an error in the 3-dB high pass corner, especially if that 3-dB corner is at a very low frequency. This statement will be proved further in Chapter II when we discuss biquad implementations of large time constants. Thus the error (in the corner) would be greater in a bi-quad. Nevertheless, the Fleischer-Laker biquad can achieve wide band operation. Indeed, the Fleischer-Laker biquad is widely used in single ended applications where DC offset is a problem. In differential ended applications, these offsets are largely eliminated by the common mode feedback circuitry.

2. *First order sections*: A high pass corner can be achieved, by designing a low pass filter with the same low pass corner as the desired high pass corner and then subtracting from a buffer or a gain stage as illustrated in the equations below

$$H_{LPF}(s) = \frac{1}{1 + s/\rho}$$

$$H_{HPF}(s) = 1 - H_{LPF}(s) = \frac{s}{s + \rho}. \quad (1.1)$$

If by some way, we could build a first order high pass section, we could eliminate the buffer or the gain stage and thus save power. This provides our motivation for coming up with a new scheme to realize large time constants in high pass sections.

## CHAPTER II

### OTA DESIGN

#### **2.1 Operation in Weak Inversion**

Biomedical applications are very low frequency applications. Thus the operational transconductor amplifiers (OTAs) used in switched-capacitor circuits for such applications have a much greater amount of time for settling. For this reason, the transistors in biomedical applications operate in weak inversion and carry currents in the nano-ampere range. Usually, the OTA power requirements in switched-capacitor applications are set by the required DC gain as well as the unity gain frequency. However, for biomedical applications, one further consideration comes into play. Transistors operating in weak inversion for biomedical applications must carry a minimum current regardless of the DC gain or settling time requirements. The reason for this is mentioned below.

Transistor currents are quite hard to control as they get smaller and smaller. The reason for this is that a large biasing resistor is required to set the biasing currents. Large resistors inject greater noise and also have lower tolerances. Thus, the biasing resistor cannot be allowed to get arbitrarily large.

The other consideration comes from the digital circuitry. Most pacemakers have analog and digital circuitry on the same chip (true mixed signal product). This makes the analog circuitry quite susceptible to substrate coupling from the digital circuitry. This coupling could momentarily cause spikes in the current flowing in the transistors in the

OTA. If the current is small enough, it could even momentarily disappear and heavily impact settling of the OTAs. Thus, a large enough bias current provides a good degree of protection from such coupling.

Finally, the matching between transistors also deteriorates with decreasing current flowing through them.

For all these reasons, the biomedical industry requires that at least 10nA of bias current flows through all transistors. More current might be required depending on settling requirements, or DC gain or noise. But 10nA is the *minimum* bias current that must flow in any transistor for such applications.

In weak inversion operation, the I-V characteristics of the MOS transistor are given by equation (2.1) [1].

$$\begin{aligned}
 I_D &= I_{D0} \frac{W}{L} (e^{(V_G - V_{TH})/\eta V_T}) [e^{-V_S/V_T} - e^{-V_D/V_T}] \\
 V_{GS} &< V_{TH} + 2\eta V_T \\
 V_{DS} &> 3V_T.
 \end{aligned} \tag{2.1}$$

Assuming  $V_S=0$  and  $V_D \gg \eta V_T$ , the equation above can be simplified as

$$\begin{aligned}
 I_D &= I_{D0} \left( \frac{W}{L} \right) e^{(V_{GS} - V_{TH})/\eta V_T} \\
 V_{DS} &> 3V_T \\
 V_{GS} &< V_{TH} + 2\eta V_T.
 \end{aligned} \tag{2.2}$$

From the equation above the trans conductance can be derived as

$$g_m = \frac{I_D}{\eta V_T}. \tag{2.3}$$

Characterization of long channel as well as short channel transistors gives us a value of around 25-45 mV for  $\eta V_T$ . The equations (2.1)-(2.3) above do not model the output resistance of the transistor. The output resistance due to channel length modulation by the drain-source voltage may be expressed in terms of an extrapolated voltage by

$$r_o = \frac{V_A}{I_D}. \quad (2.4)$$

$V_A$  can be referred to as the early voltage.

While the above equations are highly simplified, they greatly aid in design analysis. One can also expect a 20% variation in  $g_m$  and a greater variation in the output resistance from the above equations.

## 2.2. The Folded-Cascode OTA

Folded-cascode OTAs [11] are popular in switched-capacitor circuits because of their large DC gain and the fast settling time. One such structure is shown in Fig. 2-1. The large DC gain comes from the output stage that is a stack of a common source transistor (M5) and a common gate transistor (M4). Folded-cascode OTAs have a dominant pole at the output and have very good phase margin that allow them to be analyzed as single-pole systems. The good phase margin and absence of any pole-zero pair means that its transient step response has remarkably low ringing. The OTA has a p-channel input pair, which is preferred to an n-channel input pair because of the lower flicker noise of p-channel devices and also the absence of the bulk-effect.



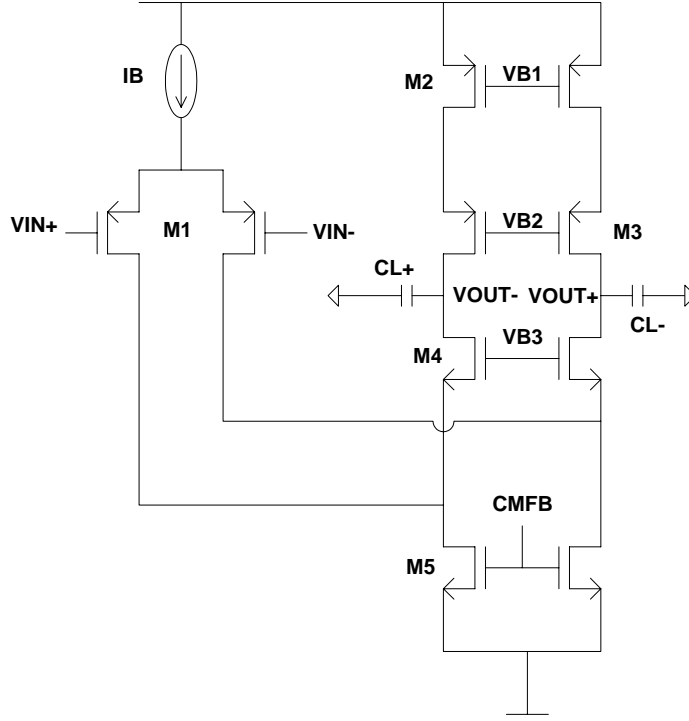


Fig. 2-1: Conventional fully differential folded-cascode OTA

The various parameters of the Folded-cascode OTA are given by equation (2.5).

$$\begin{aligned}
 A &= g_{m1}(g_{m4}r_{o4}r_{o5} \parallel g_{m3}r_{o3}r_{o2}) \\
 GBW &= \frac{g_{m1}}{C_L} \\
 v_{n,in\_thermal}^2 &= \frac{2kT\gamma}{g_{m1}} \left( 1 + \frac{g_{m5}}{g_{m1}} + \frac{g_{m2}}{g_{m1}} \right) \\
 swing &\leq V_{DD} - V_{SS} - 4V_{DS,SAT} \\
 slew &= \frac{I_B}{C_L}.
 \end{aligned} \tag{2.5}$$

The OTA may consume a minimum of 40nA of current (not counting the biasing circuitry). For this minimum power, and a supply of 1.6V, a  $g_m$  of 0.25uA/V and a DC gain of 74 dB are obtained quite easily. As will be seen later, these parameters are enough for almost all of our applications. For instance, a DC gain of 74dB results in less than 1% steady state error for capacitor ratios up to 50. A  $g_m$  of 0.25uA/V can tolerate capacitor loads of up to 10pF for less than 1% settling error for the given clock frequency.

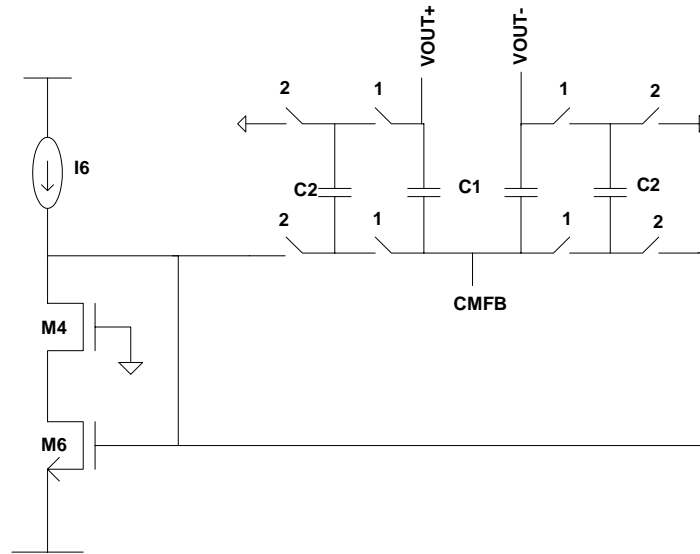


Fig. 2-2: Switched-capacitor CMFB Circuit

The structure in Fig. 2-1 is fully differential. Therefore a common mode feedback circuit is required. The switched-capacitor common-mode feedback circuit used is shown in Fig. 2-2 [10].

The output of the circuit is the node labeled CMFB. This voltage is applied to the gates to transistors M5 in Fig. 2-1. M6 (of Fig. 2-2) is similar in geometry to M5 (of Fig. 2-1) by matching. M6 generates the nominal CMFB voltage. The relation between M5 and M6 is given by

$$\frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_6} = \frac{I_{5,nom}}{I_6}. \quad (2.6)$$

Finally, note that the CMFB circuit is a discrete time circuit. Its z-domain transfer function is given by equation (2.7) below

$$\frac{V_{CMFB}(z)}{V_{O,CM}(z)} = \frac{C_2}{C_1} \frac{1}{1 - z^{-1} + \frac{C_2}{C_1}} \quad (2.7)$$

$$V_{O,CM} = \frac{V_{OUT}^+ + V_{OUT}^-}{2}.$$

$V_{O,CM}$  is the output common mode voltage of the OTA. To analyze the complete CMFB loop, we need to convert the z-domain representation to an s-domain representation. Note that such an approximation will always be crude owing to the fact the CMFB circuit is expected to settle at a speed that is comparable to the clock frequency. However, such an approximation provides us with some insight into the issues involved in designing the CMFB network. The approximate s-domain representation is given by equation (2.8)

$$\frac{V_{CMFB}(s)}{V_{O,CM}(s)} = \frac{1}{1 + \frac{s}{f_{clk}} \frac{C_1}{C_2}}. \quad (2.8)$$

The CMFB loop gain is given by

$$loop\_gain = \frac{g_{m5}}{s(C_L + C_1 + C_2) + \left( \frac{g_{o4}g_{o5}}{g_{m4}} + \frac{g_{o3}g_{o2}}{g_{m3}} \right)} \times \frac{1}{1 + \frac{sC_1}{f_{clk}C_2}}. \quad (2.9)$$

To improve stability, one could increase  $C_L$ , or  $C_2$ . Increasing  $C_L$  will push the dominant pole to a lower frequency, while increasing  $C_2$  would push the dominant pole to a lower frequency and the non-dominant pole to a higher frequency. To increase speed, one could increase  $g_{m5}$ .

### 2.3 The Single-Stage OTA

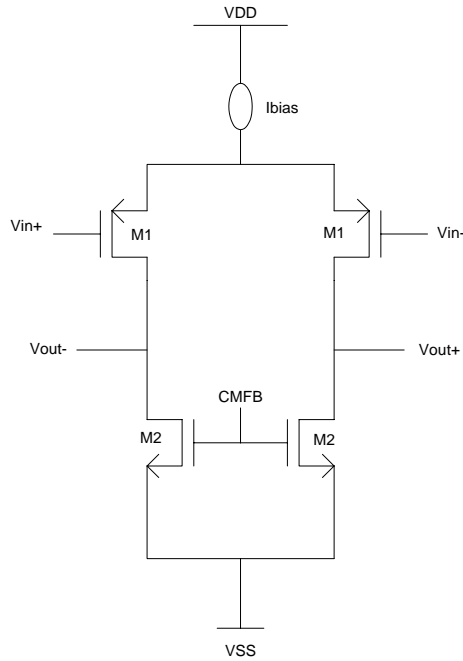


Fig. 2-3: Conventional fully differential single-stage OTA

Folded cascode OTAs provide very high gain, but for some applications like buffering, such high gains are not required. In such cases, a single stage OTA is good enough. The schematic such an OTA is shown in Fig. 2-3.

The minimum power consumption of such an OTA may be as low as 20nA following the rule that each transistor must carry at least 10nA of current. The various parameters of this OTA are:

$$\begin{aligned}
 A &= \frac{g_{m1}}{g_{o1} + g_{o2}} \\
 GBW &= \frac{g_{m1}}{C_L} \\
 slew &= \frac{I_{BIAS}}{C_L} \\
 v_{n,in}^2 &= 2 \times \frac{4kT\gamma}{g_{m1}} \left( 1 + \frac{g_{m2}}{g_{m1}} \right) \\
 V_{OUT,SWING} &= |V_{DD}| + V_{TH1} - |V_{DS,sat2}|.
 \end{aligned} \tag{2.10}$$

For a 40nA current and at the supply of 1.6V, this OTA gives us 40 dB of DC gain and  $g_m$  of 0.25uA/V. This OTA has lower power than a folded-cascode OTA and since buffering does not require a very high DC gain, this OTA is most suitable for buffering.

## 2.4 Mismatches in OTA Transistors

In differential ended structures like in Fig. 2-1 to Fig. 2-3, we do not need to worry about systematic offsets (biasing). However, random offsets could be a problem. We assume that each pair of transistors labeled M1 –M5 are perfectly matched. Under such conditions, there are no differential offsets. However, in real OTAs, offsets are always a

problem. All random offsets are a result of such mismatches between transistors or capacitors that are ideally perfectly matched. Such mismatches lead to differential offsets that could become very critical, as the time constants get larger. This will be demonstrated in succeeding chapters. The offset can be solved by a technique known as chopper stabilization [10] that basically just swaps the asymmetrical signal paths. Chopper stabilization is illustrated in Fig. 2-4 below.

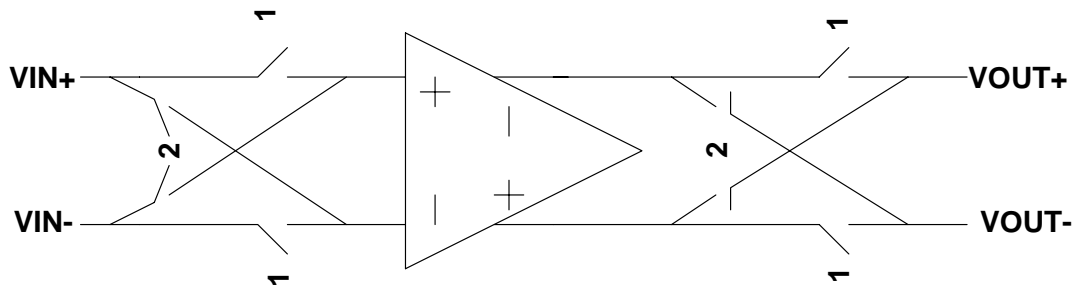


Fig. 2-4: Chopper stabilization to chop the OTA offsets to higher frequencies

The switches are controlled by a chopper clock, whose frequency (chopping frequency) is typically an even multiple of the switched-capacitor clock frequency. The chopping action is very much like the action of a mixer in RF circuits. The offsets as well as  $1/f$  noise is up converted to the chopping frequency. Assume that we have  $1/f$  noise in the bandwidth from 1 Hz to 10Hz. If the chopping clock runs at 1KHz, then the noise is up converted to a frequency bandwidth between 1001 Hz and 1010 Hz. Thus offsets can be taken care of by a chopper clock.

However, chopper stabilization leads to increased swing at both the output nodes of the OTA. This leads to greater settling time and hence greater power consumption.

Fig. 2-5 illustrates chopping action for a DC output.

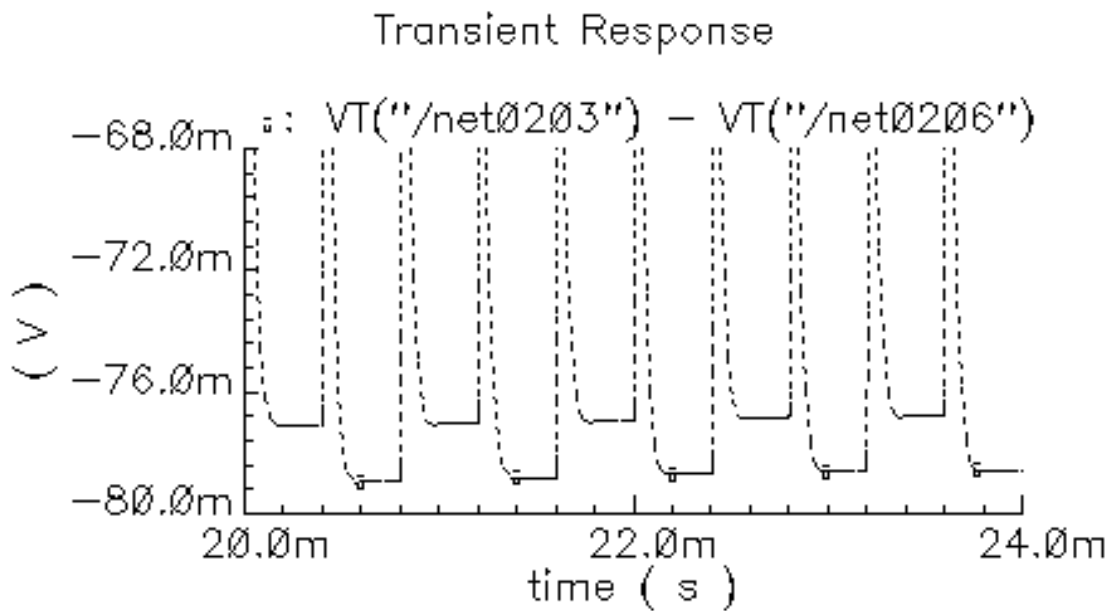


Fig. 2-5: The effect of chopper stabilization on an ideally stationary output

There is another non-ideality introduced by mismatches in the CMFB circuit. Refer back to Fig. 2-2. Lets consider what happens if the capacitors labeled C1 are not equal. Let us also assume that the capacitors labeled C2 are also not equal. Let us further assume that the ratio  $C_2/C_1$  is matched. In this case the total load capacitance at the two differential outputs of the OTA is mismatched causing a mismatch in the dominant pole frequency. This causes a pole-zero doublet, which could introduce common mode

ringing. This effect can be minimized by careful matching and cannot be removed by chopper stabilization.

## **2.5 Conclusions**

The minimum power consumption in the OTA is set by requirements such as controllability of bias currents, substrate coupling and matching. Thus, a minimum of 10nA of bias current must flow through each transistor. Thus, a folded-cascode OTA may have power consumption not lower than 40nA. This current, though small provides an OTA with enough  $g_m$  and DC gain so that up to certain values of the capacitor size, the power consumption of the OTA is independent of the loading effect on the OTA. Therefore, even though high pass filters load the OTA more than low pass filters, they do not increase the power consumption up to a certain value of time constants.



## CHAPTER III

### LARGE TIME CONSTANTS IN SC CIRCUITS

#### 3.1 Conventional Integrator

If conventional switched-capacitor (SC) structures are used to implement large time constants, the required capacitor ratios tend to be huge enough to occupy a large area thus preventing on-chip implementation. To illustrate this consider the conventional lossless integrator shown in Fig. 3-1 below [9].

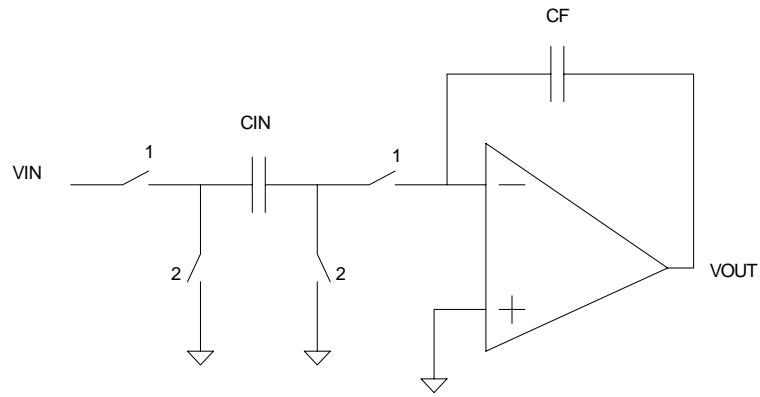


Fig. 3-1: Conventional SC lossless integrator

When the output of the integrator is taken in phase 1, the z-domain transfer function is given by

$$\frac{V_{OUT}(z)}{V_{IN}(z)} = -\frac{C_{IN}}{C_F} \frac{1}{1 - z^{-1}}. \quad (3.1)$$

The relationship between the time constant and clock frequency for such an integrator can be approximately given by equation (3.2).

$$\tau = \frac{C_f}{f_{CLK} C_{in}}. \quad (3.2)$$

If large time constants are desired, two options are available, decreasing the clock frequency or increasing the  $C_F/C_{IN}$  ratio. Decreasing the clock frequency is not really an option because we want to realize a wideband band pass function with a low pass corner at 200Hz. To prevent pre-warping errors, the clock frequency should be at least one order of magnitude larger than the low pass corner. Thus, the clock frequency is limited by the low pass corner we want to achieve. This leaves us with the option of increasing the  $C_F/C_{IN}$  ratio. The required capacitor spread can easily run into a several hundreds or even a few thousands in practice. For instance, a 1Hz high pass corner working from a 2.5 KHz clock would require a capacitor spread of around 400.

Several approaches have been investigated for realizing very large time constants in an area efficient manner. Most of these approaches achieve the required capacitor ratio as a product of two smaller capacitor ratios. For instance, if a capacitor spread of 400 can be realized as a product of two capacitor ratios of 20 each. Thus the total area has been reduced by a factor of 10 in the above case. In subsequent sections, we will discuss the various techniques by which this is achieved. For each of the techniques, we will demonstrate capacitor spread, capacitor area, the effects of op-amp DC gain and GBW, the sensitivity to capacitor mismatch, sensitivity to op-amp mismatches (differential mode offsets). We will do this for the extremes of the corner frequency, viz. 4Hz and 0.159 Hz.

### 3.2 Fleischer-Laker (FL) Biquad

The Fleischer-Laker biquad [8] is a wideband low-Q biquad. It consists of a two integrator loop, one lossy and one lossless. The switched-capacitor implementation is shown in Fig. 3-2 below.

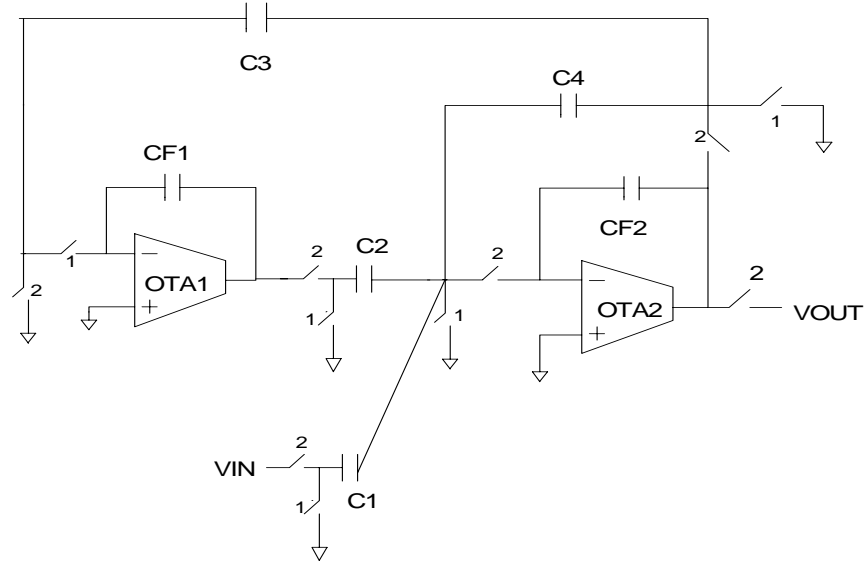


Fig. 3-2: Conventional Fleischer-Laker biquad for low Q applications

The output of OTA 1 is a low pass function and the output of OTA 2 is the required wideband band pass function. The z-domain transfer function is given by

$$\frac{V_{OUT}(z)}{V_{IN}(z)} = -\frac{C_1}{C_{F2}} \frac{1 - z^{-1}}{(1 - z^{-1})^2 + \frac{C_4}{C_{F2}}(1 - z^{-1}) + \frac{C_2 C_3}{C_{F1} C_{F2}} z^{-1}}. \quad (3.3)$$

To analyze approximately for the corners, the z-domain representation must be converted to an s-domain representation. This is not necessary, but since we are more

used to dealing in the continuous-time, it is more convenient. The universal transformation is given by

$$z^{-1} \leftrightarrow e^{-sT_{clk}}. \quad (3.4)$$

$T_{CLK}$  is the sampling clock frequency. This is a nonlinear transformation and can lead to cumbersome expressions sometimes. If the clock frequency is sufficiently higher than the operating frequency of the SC filter, then a bi-linear transformation can be used. The transformation can be approximated by

$$\begin{aligned} z^{-1} &= \frac{1 - 0.5sT_{CLK}}{1 + 0.5sT_{CLK}} \\ z^{-1/2} &= \frac{\sqrt{1 - s^2T_{CLK}^2}}{1 + 0.5sT_{CLK}} \approx \frac{1}{1 + 0.5sT_{CLK}}. \end{aligned} \quad (3.5)$$

A few more approximations are in order to derive a less cluttered expression and develop insight.

$$\frac{C_2C_3}{C_{F1}C_{F2}} \ll \frac{C_4}{C_{F2}}. \quad (3.6)$$

This transformation will give us an accurate result for the high pass corner, which is low frequency, but it will give some error for the low pass corner (a large value). Using the above transformation, we obtain

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = -\frac{C_1}{C_{F2}} \frac{sT_{CLK}(1 + 0.5sT_{CLK})}{s^2T_{CLK}^2(1 + \frac{C_4}{2C_{F2}}) + s\frac{C_4}{C_{F2}}T_{CLK} + \frac{C_2C_3}{C_{F1}C_{F2}}(1 + 0.5sT_{CLK})}. \quad (3.7)$$

For obtaining the high pass corner, which is at low frequency, we can make one further approximation, i.e.  $1 + 0.5sT_{CLK} \approx 1$ . This will give us

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{s \frac{2C_1}{2C_{F2} + C_4} f_{clk}}{s^2 + s \frac{2C_4}{C_4 + 2C_{F2}} f_{clk} + \frac{2C_2 C_3}{C_{F1}(C_4 + 2C_{F2})} f_{clk}^2}. \quad (3.8)$$

In the above transfer function, the roots of the denominator (or the poles of the transfer function) will give us the approximate high pass and low pass corners. The corners can be derived as

$$\begin{aligned} \rho_{HPF} &= f_{clk} \frac{C_2 C_3}{C_4 C_{F1}} \Rightarrow \tau_{HPF} = \frac{C_4 C_{F1}}{C_2 C_3 f_{clk}} \\ \rho_{LPF} &= f_{clk} \frac{2C_4}{(C_4 + 2C_{F2})} \Rightarrow \tau_{LPF} = \frac{2C_{F2} + C_4}{2f_{clk} C_4} \\ G(passband) &= \frac{C_1}{C_4}. \end{aligned} \quad (3.9)$$

The derived high pass corner is much more accurate than the derived low pass corner. For greater accuracy in deriving the low pass corner, we need to pre warp the low pass corner. We can thus obtain the more accurate low pass corner as in [8]

$$\rho_{LPF} = \frac{f_{clk} \frac{2C_4}{2C_{F2} + C_4} \sin\left(\frac{2C_4}{2C_{F2} + C_4}\right)}{\frac{2C_4}{2C_{F2} + C_4}} = f_{clk} \sin\left(\frac{2C_4}{2C_{F2} + C_4}\right). \quad (3.10)$$

Thus, the problem of realizing the large time constant has been solved by now involving four capacitors rather than just two in conventional switched-capacitor structures. From the above equations a few facts are clear:

1.  $C_4 < C_{F2}$  because the clock is one order higher than the low pass corner
2.  $C_4$  and  $C_{F1}$  are much larger than  $C_2, C_3$  for large time constants

3.  $C_1$  is as large as  $C_4$  if a gain of 1 is desired and larger for larger gains

### 3.2.1 Capacitors, matching and sensitivity

$C_4$ ,  $C_2$ ,  $C_1$  and  $C_{F2}$  must be mutually matched, as must  $C_3$  and  $C_{F1}$ . Since  $C_2$  and  $C_3$  are the only small capacitors in their respective cluster, both can be unit capacitors for common centroid matching to be possible. The capacitor values are given in Table 3-1. The low pass corner is always fixed at 200Hz. The values have been optimized for spread. They can also be optimized for GBW as will become clear in the discussion in section 3.2.3.

Table 3-1: Capacitor values for FL biquad of Fig. 3-2

$f_{HPF}$	$C_1$	$C_2$	$C_3$	$C_4$	$C_{F1}$	$C_{F2}$
0.159 Hz	36	1	1	36	70	70
4 Hz	8	1	1	8	14	14

The capacitor spreads depend on both the high pass and the low pass corner. While having a small high pass corner causes a large capacitor spread, the presence of a low pass corner pushes the spreads to even higher values. This is one disadvantage of this biquad.

The sensitivities with respect to all capacitor mismatches have a magnitude of 1. As an example for calculation, let us calculate the sensitivity of the high pass corner with respect of  $C_{F1}$ .

$$S_{C_{F1}}^{\rho_{HPF}} = \left( \frac{\partial \rho_{HPF}}{\partial C_{F1}} \right) \div \frac{\rho_{HPF}}{C_{F1}} = -1. \quad (3.11)$$

Similarly it can be shown that the sensitivity with respect to  $C_2$  and  $C_3$  is 1 while the sensitivity of the high pass corner with respect to  $C_4$  is -1. Thus the absolute value of sensitivity with respect to all capacitors is 1. The absolute sensitivity is given by

$$S = \left| S_{C_{F1}}^{\rho_{HPF}} \right| + \left| S_{C_2}^{\rho_{HPF}} \right| + \left| S_{C_3}^{\rho_{HPF}} \right| + \left| S_{C_4}^{\rho_{HPF}} \right| = 4. \quad (3.12)$$

### 3.2.2 Effects of finite DC gain

The ideal transfer function in a Fleischer-Laker biquad has a zero at the origin and two left half poles in the s-plane for a continuous time implementation. For a discrete time implementation, the zero ideally lies on the unit circle and the poles lie within the unit circle of the z-plane. This is true if the op-amps are ideal. However, if the op-amp is not ideal, then the transfer function contains a zero inside the unit circle (analogous to a left half zero). This causes not only a phase error, but also an error in the 3-dB high pass corner. The main reason for this zero is that a lossless integrator if implemented by a non-ideal op-amp is actually lossy. The larger the gain of the op-amp, the smaller the loss. The transfer function considering finite DC gain is given by

$$\begin{aligned}
H(z) &= -\frac{C_1}{C_{F2}(1+A_2^{-1})} + \frac{1-z^{-1} + \frac{C_3}{(1+A_1)C_{F1}}}{(1-z^{-1})^2 + G_1(1-z^{-1}) + G_2z^{-1/2}} \\
G_1 &= \frac{C_4}{C_{F2}} + \frac{C_1}{C_{F2}(A_2+1)} + \frac{C_3}{C_{F1}(A_1+1)} \\
G_2 &= \frac{C_2C_3}{C_{F1}C_{F2}(1+A_1^{-1})(1+A_2^{-1})}.
\end{aligned} \tag{3.13}$$

The frequency of the zero is given by

$$\rho_z = \frac{f_{clk}C_3}{A_1C_{F1}}. \tag{3.14}$$

For small DC gains, this zero can be uncomfortably close to the required high pass corner. For instance, in the biquad above, if OTA 1 has a DC gain of 40 dB (normal for a current mirror OTA), then the zero frequency is only three times lower than the frequency of the required pole. By increasing the spread, the zero can be pushed to lower frequencies, but the spreads are already too high. Thus, OTA 1 must have a large DC gain. A typical folded-cascode (gain = 74 dB) can push the zero to reasonably lower frequencies, so that it does not affect the response too much.

Another error is due to the apparent change in the values of  $C_{F1}$ ,  $C_{F2}$  and  $C_4$ . This change is entirely due to the DC gain. The apparent values become

$$\begin{aligned}
C_{F1} &\rightarrow C_{F1}(1+A_1^{-1}) \\
C_{F2} &\rightarrow C_{F2}(1+A_2^{-1}) \\
C_4 &\rightarrow C_4(1+A_2^{-1}).
\end{aligned} \tag{3.15}$$

These errors are quite obvious from inspection. These errors are quite small however. The point that we are trying to make here is that one has to use large DC gain



to realize the required transfer function with a reasonable accuracy. These conclusions can be verified via simulations.

### 3.2.3 Op-amp GBW

OTA 1 is effectively loaded by capacitor  $C_3$  during phase 1 and  $C_2$  during phase 2. Both of these are small capacitors and hence OTA 1 has minimal GBW requirements. OTA 2 however is loaded by a parallel combination of  $C_1$ ,  $C_2$  and  $C_3$  during phase 2. The loading diagrams for OTA 2 are shown below in Fig. 3-3a and Fig. 3-3b.

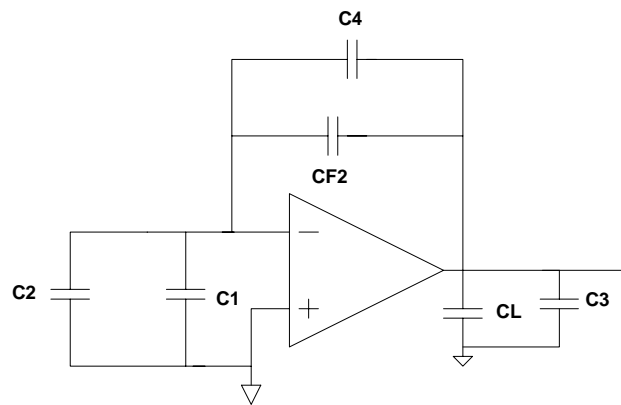


Fig. 3-3a: Loading configuration for OTA 2 of Fig. 3-2 during phase 2

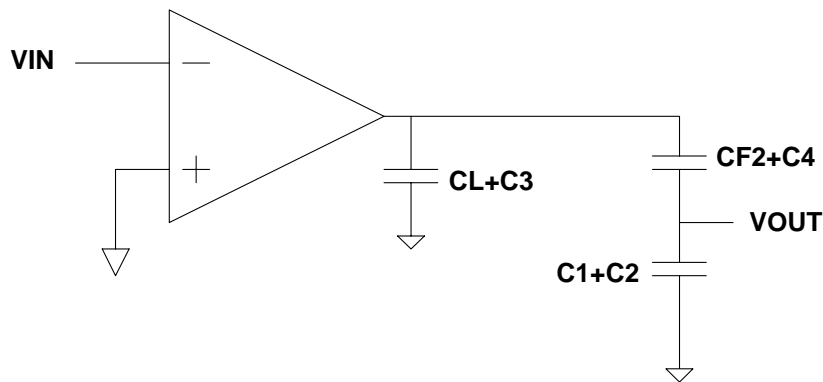


Fig. 3-3b: Circuit of Fig. 3-3a with feedback loop opened

The loop GBW is given by

$$loop\_GBW = \frac{g_m}{C_1 + C_2 + (C_L + C_3) \left( 1 + \frac{C_1 + C_2}{C_{F2} + C_4} \right)}. \quad (3.16)$$

$C_1$  is a big capacitor and loads the OTA, impacting settling time. Thus, as the time constants increase and push up the spread,  $C_1$  increases and thus OTA 2 requires greater power consumption ( $g_m$ ) for proper settling.

### 3.2.4 Op-amp offsets

One advantage of the Fleischer-Laker biquad is that it is robust with respect to op-amp offsets. This is why, in single ended implementations of large time constants, the FL biquad is preferred over other methods. For differential ended structures, this advantage vanishes because of the very nature of differential ended circuitry. In differential ended circuits, the biasing offsets (systematic offsets) appear as a common mode voltage, which is eliminated by the common mode feedback circuitry. Mismatch offsets (random offsets) can be eliminated by chopper stabilization. The output offset of the FL biquad is approximately equal to (but of opposite sign) the input referred offset of the OTA 1. This can be intuitively seen by understanding that in steady state, no charge flows through either integrating capacitor  $C_{F1}$  or  $C_{F2}$ . Thus,

$$V_{out,off} = -V_{in,off,OTA1}. \quad (3.17)$$

### 3.3 The T-Cell Method [4]

To understand the T-Cell method, consider the discrete time integrator in Fig. 3-4. To achieve a large time constant  $C_{IN}$  needs to be as small as possible and  $C_F$  should be as large as possible. Conceptually, this can be achieved by placing an attenuator between the input and  $C_{IN}$  and/or an amplifier between the output and  $C_F$ . The conceptual schematic is shown below in Fig. 3-4.

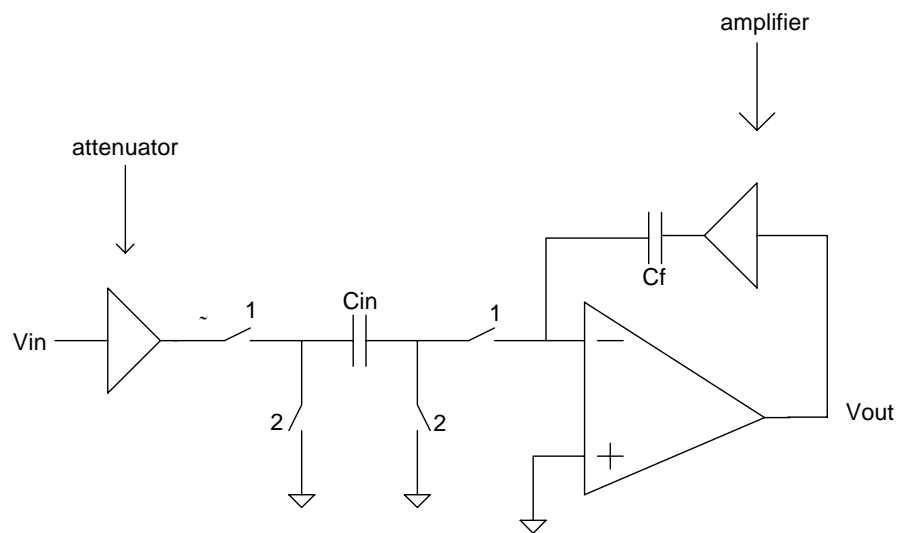


Fig. 3-4: Conceptual implementation of large integrator time constants

Thus the input signal is reduced by an attenuating factor ( $>1$ ) and the feedback signal is increased by the amplification factor ( $>1$ ). Thus, the time constant of the integrator increases by the product of the attenuation and amplification factors. The effect is equivalent to reducing the input capacitor,  $C_{in}$  (increasing the resistor) and increasing the feedback capacitor  $C_F$  (the integrating capacitor). Amplification can be implemented only by adding an extra OTA. This increases power consumption.

Attenuation does not need active elements. Passive voltage division can implement it. This is the theory behind the T-Cell implementation. The T-Cell method implements a small input capacitor by means of capacitive (switched capacitive) voltage division. The switched-capacitor implementation of the T-Cell integrator is shown in Fig. 3-5.

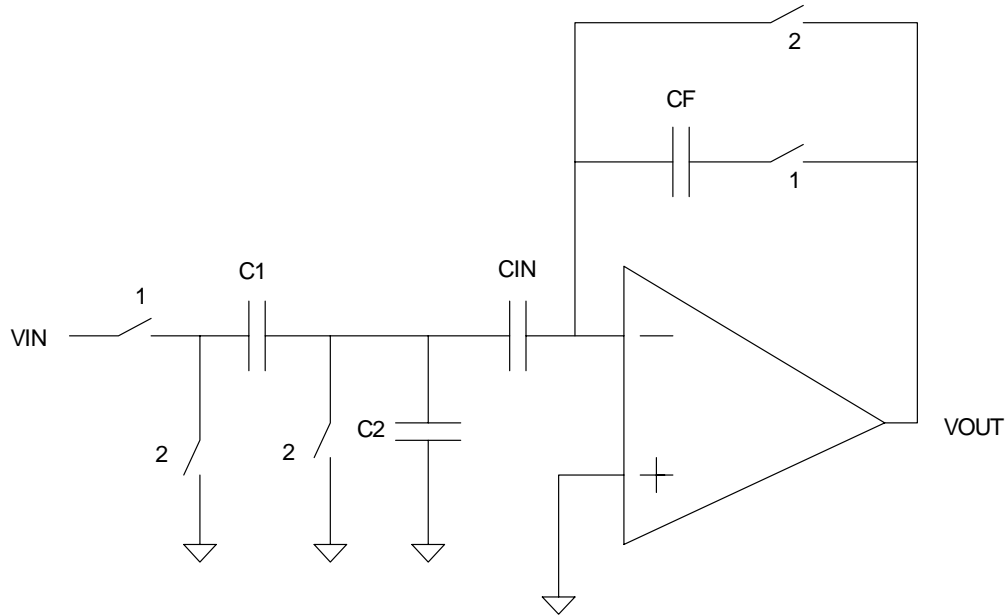


Fig. 3-5: Large TC integrator using the T-Cell technique

$C_1$  and  $C_2$  make sure that only a small fraction of the input charge is actually integrated by passage through  $C_F$ . The z-domain transfer function, when the output is sampled in phase 1 is given by

$$\frac{V_o(z)}{V_{in}(z)} = -\frac{C_1}{C_1 + C_2 + C_{IN}} \frac{C_{IN}}{C_F} \frac{1}{1 - z^{-1}}. \quad (3.18)$$

To implement a lossy integrator using the T-Cell, one will have to use it in the Fleischer-Laker biquad. This structure is not parasitic-insensitive. When using poly

capacitors, the bottom plate parasitic capacitor could be as large as 20% of the main capacitor. Metal-Metal capacitors have smaller parasitic effects, but they occupy a huge amount of chip area compared to poly capacitors. Therefore, we will not be using this structure or discussing it further.

### 3.4 The Split-Integrating Capacitor Technique [3]

Consider the lossless integrator again. The T-Cell technique was concerned with making the input capacitor look small. The split-integrator technique uses the same principle, but the implementation is parasitic-insensitive. The way it does this is by throwing away a big fraction of the input charge and only passing a small fraction of it through the feedback integrating capacitor. The conceptual diagram is shown in Fig. 3-6.

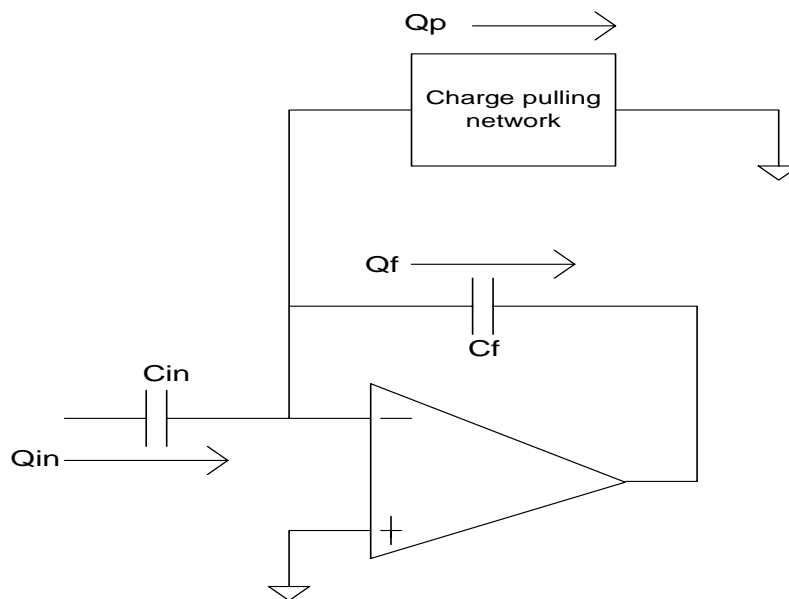


Fig. 3-6: Conceptual diagram of the split-integrating capacitor technique

In the conventional integrator, the whole of the input charge passes through the integrating feedback capacitor. In the split-integrating technique, a considerable fraction of the input charge is sucked in by the charge pulling network and only a small fraction of the input charge passes through the integrating feedback capacitor. This operation makes the feedback capacitor look much larger than it actually is or conversely, we can say that it makes the input capacitor look small.

Fig. 3-7 demonstrates the discrete time implementation of the technique. The feedback capacitor  $C_F$  is split into three capacitors,  $C_{F1}$ ,  $C_{F2}$  and  $C_{F3}$ . The circuit exploits an extra op-amp phase. In the conventional integrator, the integration and sampling are performed only in phase 1. In phase 2, the op-amp is idle and the output is a don't care. In the split-integrator technique, both phases are used. In phase 1, the input charge ( $Q_{in} = C_{in}V_{in}$ ) is divided between  $C_{F1}$  and  $C_{F2}$ . In phase 2, the bigger capacitor,  $C_{F1}$  discharges to ground, and a significant portion of the input charge is lost. The smaller capacitor,  $C_{F2}$ , which holds only a small portion of the input charge, discharges through the integrating capacitor. Thus only a small portion of the input charge is integrated, making the integrating capacitor look really very big.

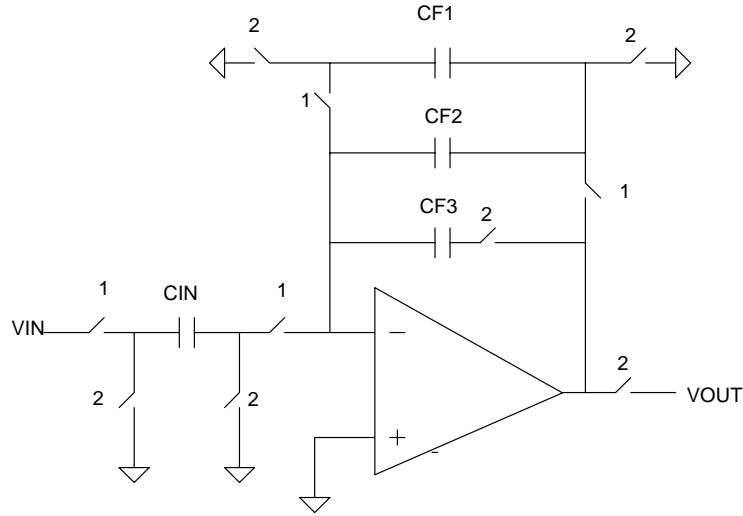


Fig. 3-7: SC implementation of the concept shown in Fig. 3-6

The z-domain transfer function can be written as

$$\frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_{F2}}{C_{F3}} \frac{C_{IN}}{C_{F2} + C_{CF1}} \frac{z^{-1/2}}{1 - z^{-1}}. \quad (3.19)$$

The relationship between the time constant and the clock frequency is given by

$$\tau = \frac{C_{F3}}{C_{IN}} \frac{C_{F2} + C_{F1}}{C_{F2}} \frac{1}{f_{clk}}. \quad (3.20)$$

Thus for a large time constant,  $C_{F3}$  and  $C_{F1}$  must be large while  $C_{IN}$  and  $C_{F2}$  must be small. Also  $C_{IN}$ ,  $C_{F2}$ ,  $C_{F1}$ ,  $C_{F3}$  must all be mutually matched.

Now, we must, at this point, begin to wonder whether a lossy integrator can be synthesized using this technique. It may be impossible to do this using only one op-amp. To implement a lossy integrator, let us go back to the conceptual diagram as given below.

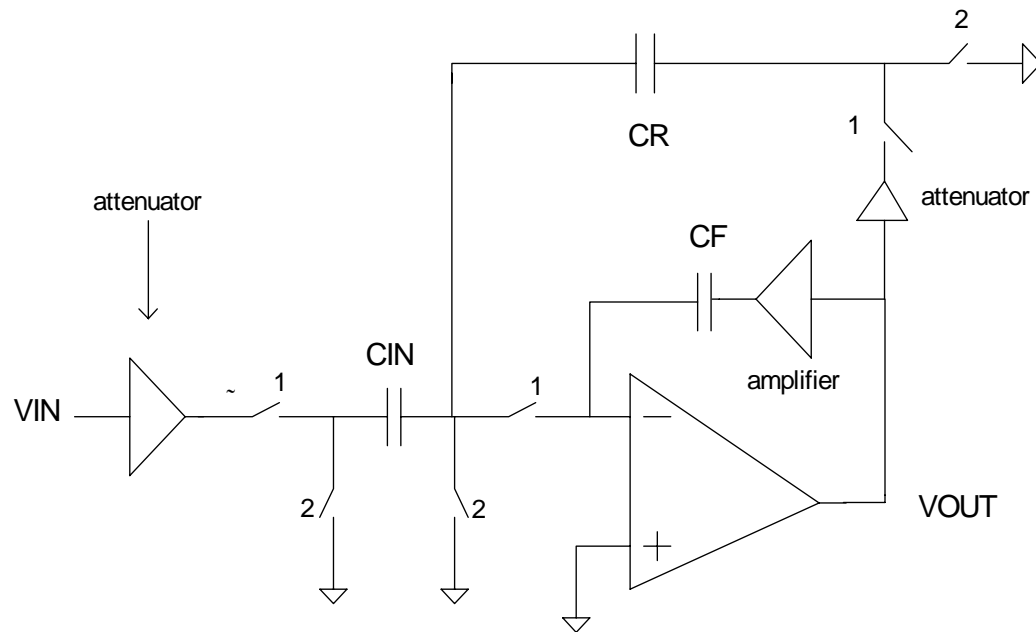


Fig. 3-8: Conceptual implementation of large TC LPF

The technique makes the input capacitor  $C_{IN}$  look small (using the attenuator). To maintain gain and also a large time constant, it must also make  $C_R$  look small. To do this, it must attenuate the output  $V_{OUT}(n)$ . Both clock phases are already utilized (one is utilized in attenuating the input signal and the other in the integration). So we would need an extra clock to make  $C_R$  look small. Thus, we cannot implement a lossy integrator, using just this one op-amp and only two clock phases. To implement a lossy integrator using this technique and only two clock phases, we will need to use this integrator in an FL biquad. The discrete-time implementation is shown in Fig. 3-9. The loop implements a high pass function. Technically, we don't need  $C_{F2}$ . I have just included it for completeness. We can allow the value of  $C_{F2}$  to be any value of our choosing, i.e. any arbitrarily small value.



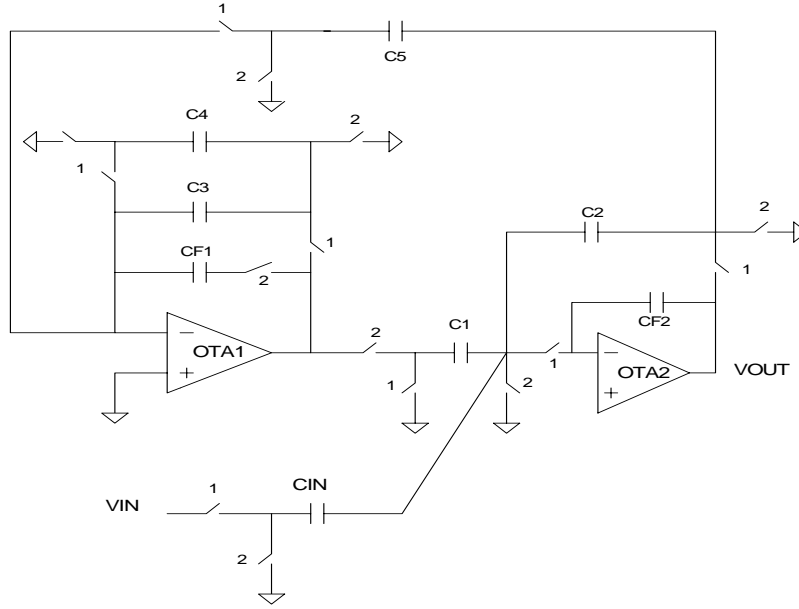


Fig. 3-9: A large time constant integrator in the FL biquad

The transfer function is given by

$$H(z) = -\frac{C_{IN}}{C_{F2}} \frac{1 - z^{-1}}{(1 - z^{-1})^2 + (1 - z^{-1}) \frac{C_2}{C_{F2}} + \frac{C_1 C_3 C_5}{C_{F1} C_{F2} (C_3 + C_4)} z^{-1}}. \quad (3.21)$$

The high pass corner is then given by

$$\rho_{HPF} = f_{clk} \frac{C_1 C_3 C_5}{C_{F1} C_2 (C_3 + C_4)}. \quad (3.22)$$

If  $C_1 = C_3 = C_5 = C$ , and  $C_{F1} = C_2 = C\beta$ , and  $C_4 = (\beta - 1)C$ , then the corner is given by equation (3.23).

$$\rho_{HPF} = \frac{f_{clk}}{\beta^3}. \quad (3.23)$$

### 3.4.2 Capacitors, matching and sensitivity

$C_5$ ,  $C_3$ ,  $C_4$ ,  $C_{F1}$  form one cluster.  $C_1$ ,  $C_{in}$ ,  $C_{f2}$  and  $C_2$  form another cluster. The various capacitor sizes are given in Table 3-2.

Table 3-2: Capacitor values for Fig. 3-9, DNM stands for does not matter

Corner	$C_1$	$C_2$	$C_3$	$C_4$	$C_5$	$C_{IN}$	$C_{F1}$	$C_{F2}$
4 Hz	1	4	2	8	2	4	5	DNM
0.159	1	14	2	26	2	14	26	DNM

The magnitude of sensitivity of the high pass corner with respect to all capacitor ratios is 1. Sensitivity is defined the same way as in section 3.2.1. However, the structure is more sensitive than first order sections or even the conventional FL biquad, because there are more ratios (3 rather than 2) involved in determining the time constant. The value of total sensitivity (as defined in B1) is 6.

### 3.4.3 Op-amp DC gain

If the finite DC gain of the op-amp is considered, the transfer function is given by equation 3.24 below.

$$H(z) = -\frac{C_{IN}}{C_{F2}} \frac{1 - z^{-1} + \frac{C_3}{C_{F1}(A_1 + 1)}}{(1 - z^{-1})^2 + (1 - z^{-1}) \left( \frac{C_3}{C_{F1}(A_1 + 1)} + \frac{C_2}{C_{F2}} + \frac{C_{IN}}{A_2 C_{F2}} \right) + G z^{-1}} \quad (3.24)$$

$$G = \frac{C_1 C_3 C_5}{C_{F1} C_{F2} (C_3 + C_4)}.$$

Just like in the conventional FL biquad, the finite DC gain of OTA moves a zero within the unit circle. The frequency of this zero is given by

$$\rho_z = \frac{C_3}{C_{F1}(A + 1)}. \quad (3.25)$$

For small gains of OTA 1, the zero is too close to the high pass corner.

#### 3.4.4 Op-amp GBW

OTA 1 is loaded by the parallel combination of  $C_5$  and  $C_1$  while OTA 2 is loaded by the parallel combination of  $C_{in}$ ,  $C_1$  and  $C_3$ . All of these are small capacitors and hence there will not be much of a problem with respect to settling even for minimum power consumption.

#### 3.4.5 Op-amp offsets

The output offset of this biquad can be shown to be equal in magnitude to the input referred offset of OTA 1. So offsets are not a problem in this biquad.

### 3.5 The Nagaraj Technique [5]

The Nagaraj technique is by far the most area efficient method of implementing large time constants yet. A circuit schematic of the Nagaraj integrator is shown in Fig. 3-10.

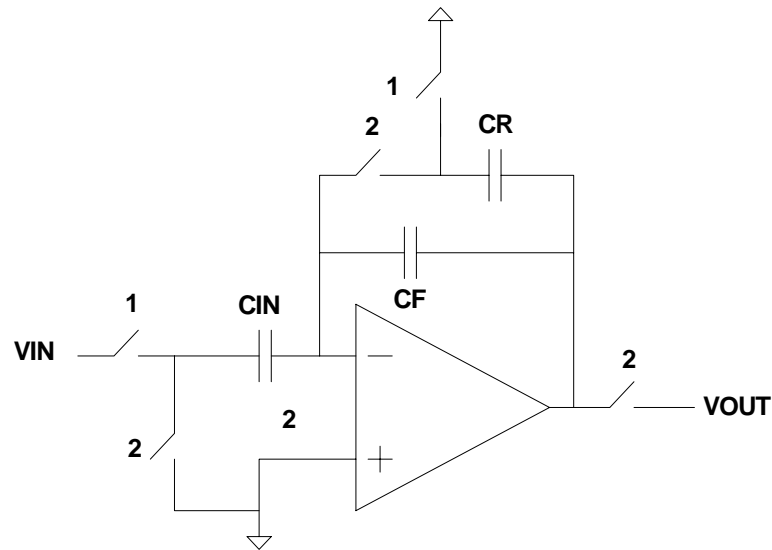


Fig. 3-10: The Nagaraj integrator

In each of the schemes discussed earlier, the basic trick has been the same. The charge passing through the integrating capacitor must be limited to as small a fraction of the input charge as possible. The Nagaraj technique is no different in this respect. However, in the techniques discussed above, attenuation and integration were performed by different capacitors. In the Nagaraj technique, the same capacitor is used to perform the integration as well as the attenuation function resulting an almost 50% saving in total capacitance. In the above circuit schematic, capacitor  $C_2$  is used for attenuation as well as for integration. This is illustrated by Fig. 3-11.

The circuit on the left illustrates the charge transfer in phase 1 while that on the right illustrates the charge transfer in phase 2. In phase 1, the entire input charge ( $Q_{IN} = Q_F$ ) flows through  $C_F$ , which is the big integrating capacitor. In phase 2, almost the entire

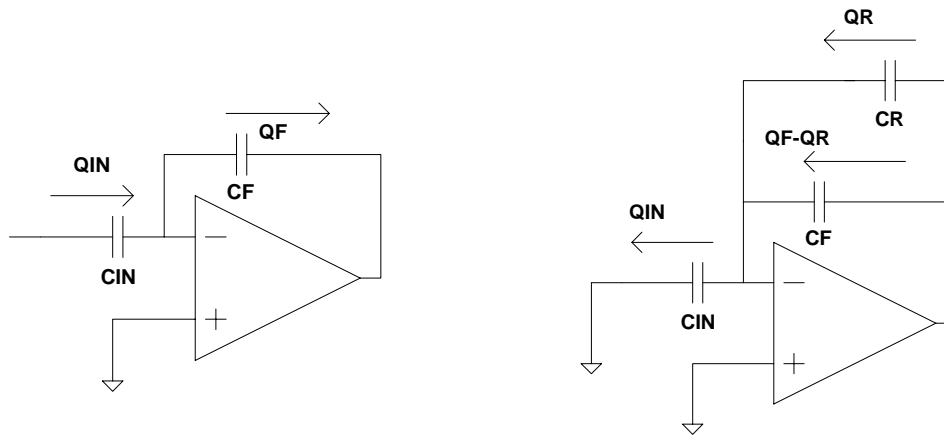


Fig. 3-11: Illustrating the integrating principle in the Nagaraj integrator

input charge ( $Q_{IN} - Q_R$ ) flows through the integrating capacitor, but in the reverse direction. Thus, in effect, only a small portion of the input charge ( $Q_R$ ) is integrated by the large capacitor  $C_F$ . Voltage waveforms are shown in Fig. 3-12.

During phase 1, the output voltage takes a step of a certain size in the negative direction. This is when the input charge flows through  $C_F$ . During phase 2, when a large fraction of the input charge is returned by  $C_F$ , the voltage waveform takes a step in the positive direction. The step in the positive direction is a little less than the one in the negative direction.

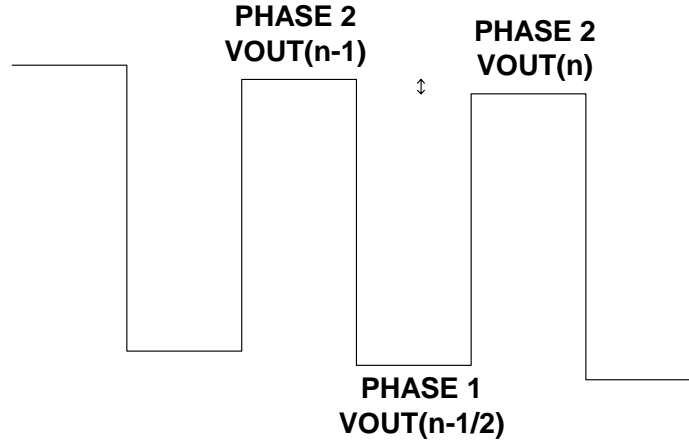


Fig. 3-12: Illustrating the voltage waveforms in the Nagaraj integrator

The z-domain transfer function of the integrator is

$$H(z) = -\frac{1}{1 + \frac{C_2}{C_F}} \frac{C_2}{C_F} \frac{C_{IN}}{C_F} \frac{z^{-1/2}}{1 - z^{-1}}. \quad (3.25)$$

The time constant of the integrator is given by

$$\tau = \left[ 1 + \frac{C_2}{C_F} \right] \frac{C_F}{C_{IN}} \frac{C_F}{C_2} \frac{1}{f_{clk}}. \quad (3.26)$$

Thus  $C_F$  is a large capacitor and  $C_{IN}$ ,  $C_2$  are small capacitors. Rather large time constants can be implemented with reasonable capacitor ratios.

The idea above can be extended to realize lossy integrators as shown in Fig. 3-13. The transfer function of the integrator can be shown to be

$$H(z) = - \frac{1}{\left(1 + \frac{C_2}{C_F}\right) \left(1 + \frac{C_1}{C_F}\right)} \frac{C_{IN}}{C_F} \frac{C_2}{C_F} \left[ \frac{z^{-1/2}}{1 - z^{-1} + \frac{1}{\left(1 + \frac{C_1}{C_F}\right) \left(1 + \frac{C_2}{C_F}\right)} \frac{C_1 C_2}{C_F^2} z^{-1}} \right] \quad (3.27)$$

The DC gain of this lossy integrator (LPF) is equal to  $C_{IN}/C_1$ .

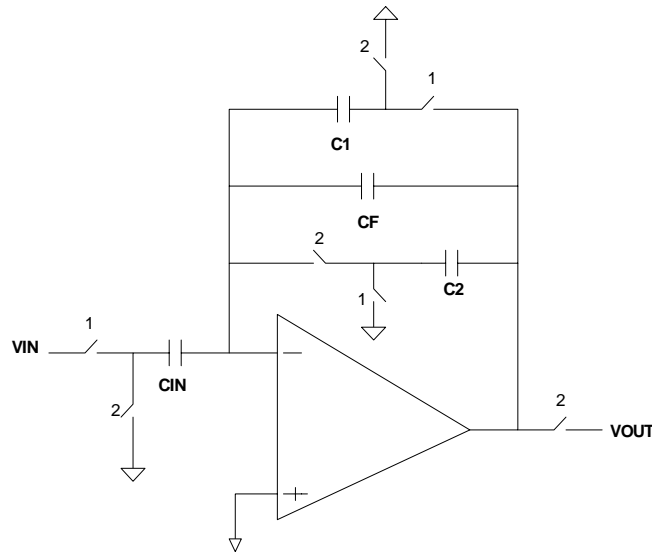


Fig. 3-13: The Nagaraj low pass filter

The corner frequency is given by

$$\rho = \frac{C_1 C_2}{C_F^2} f_{clk} \frac{1}{\left(1 + \frac{C_1}{C_F}\right) \left(1 + \frac{C_2}{C_F}\right)}. \quad (3.28)$$

Large time constants are obtained by keeping  $C_F$  large and  $C_1$ ,  $C_2$ ,  $C_{IN}$  small. Let us now analyze the Nagaraj low pass filter for various parameters.

### 3.5.2 Capacitors, matching and sensitivity

Capacitors  $C_1$ ,  $C_2$ ,  $C_{in}$  and  $C_F$  belong to the same cluster and hence must be mutually matched. Since  $C_{1,2,in}$  are all small capacitors, all three of them cannot be mutually matched and be unit capacitors at the same time. Here, we come across a tradeoff between capacitor spread and capacitor area. Given in Table 3-3 is the list of capacitor values optimizing spread. Table 3-4 optimizes area.

Table 3-3: Capacitor values for Fig. 3-13 optimizing spread

Corner	$C_{IN}$	$C_1$	$C_2$	$C_F$
0.159	2	2	2	98
4	2	2	2	18



Table 3-4: Capacitor values for Fig. 3-13 optimizing area

Corner	$C_{IN}$	$C_1$	$C_2$	$C_F$
0.159	2	2	1	70
4	2	2	1	13

The sensitivities are given by

$$\begin{aligned}
 S_{C_F}^{\rho_{HPF}} &= -2 \\
 S_{C_1}^{\rho_{HPF}} &= 1 \\
 S_{C_2}^{\rho_{HPF}} &= 1 \\
 S &= 4.
 \end{aligned} \tag{3.29}$$

The Nagaraj structure is about as sensitive as the conventional Fleischer-Laker biquad.

### 3.5.3 Op-amp DC gain

If op-amp DC gain is taken into account, the transfer function for the low-pass filter can be derived to equal the expression in equation (3.30).

$$H(z) = -\frac{C_2 C_{IN}}{C_F^2} \frac{1}{\left(1 + \frac{C_2}{C_F}\right)\left(1 + \frac{C_1}{C_F}\right)} \left( \frac{1}{1 - \left( \frac{C_1 C_2}{C_F^2} \frac{1}{\left(1 + \frac{C_2}{C_F}\right)\left(1 + \frac{C_1}{C_F}\right)} + \frac{C_1}{AC_F} \right)} - z^{-1} \right). \quad (3.30)$$

The new corner frequency is given by

$$\rho = f_{clk} \left( \frac{C_1 C_2}{C_F^2} \frac{1}{\left(1 + \frac{C_1}{C_F}\right)\left(1 + \frac{C_2}{C_F}\right)} + \frac{C_1}{AC_F} \right). \quad (3.31)$$

The error in the time constant is thus given by

$$\varepsilon = \frac{C_1}{C_1 C_2} \frac{C_F}{A}. \quad (3.32)$$

If  $C_{IN} = C_1 = C_2 = C$  and  $C_F = \beta C$ , then the error is given by

$$\varepsilon = \frac{\beta}{A}. \quad (3.33)$$

Thus for a time constant of 1s (cutoff of 0.159 Hz) and a clock of 2.5 KHz, the Spread required is 50 and the DC gain required for 1% error would be 5000 or 74dB.

### 3.5.4 Op-amp GBW

There is not much stress on the GBW of the OTA because the AC loading capacitor in both phases is  $C_{IN}$ , which is a small capacitor. The GBW requirement can be met easily by the minimum power OTA (40nA).

### 3.5.5 Op-amp offsets

The effects of the op-amp offsets can be derived in straightforward manner. The way to do this, is to set the input to zero, assume infinite DC gain and assign an input referred offset of  $V_{IN,off,OTA}$  to the OTA. The output offset can be derived to be

$$V_{out,off} = 2\beta V_{in,off,OTA}. \quad (3.34)$$

Since we are using fully differential configurations, we do not worry about biasing offsets. Mismatch offsets can be removed by chopper stabilization [10].

## 3.6. Combining the FL Biquad with the Nagaraj Integrator

We might recall that the FL biquad contained a two integrator loop of which one integrator was lossy and the other, lossless. Two of the problems, viz. large capacitor spread and area, and loading effect can be greatly alleviated, by replacing the conventional integrator with the Nagaraj integrator. Doing so reduces the area as well as the spread as compared with the first order Nagaraj lossy integrator. The switched-capacitor implementation of the improved FL biquad is shown in Fig. 3-14.

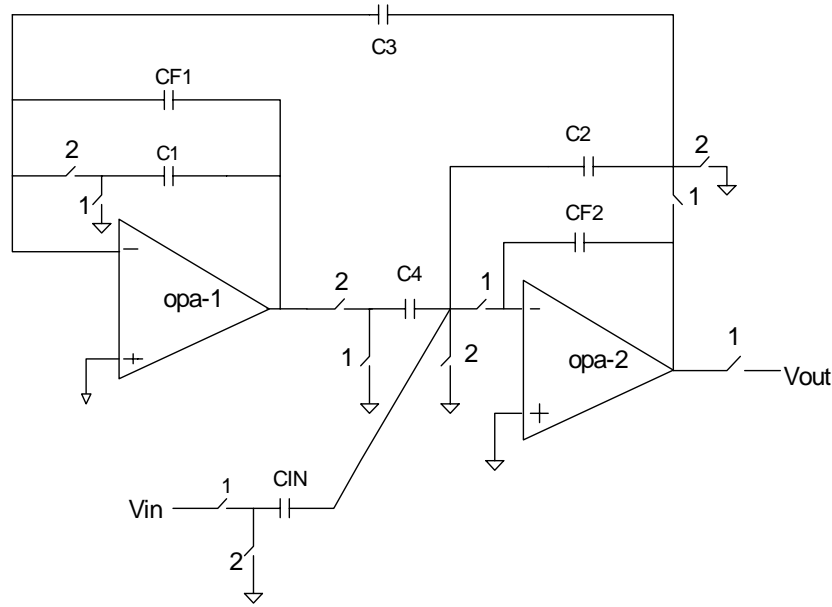


Fig. 3-14: FL biquad using the Nagaraj integrator

Opa-1 implements the lossless Nagaraj integrator while opa-2 implements the conventional lossy integrator. Recall that in the conventional FL biquad,  $C_{IN}$ ,  $C_{F2}$  and  $C_2$  would be large capacitors increasing the area as well as the loading on opa-2. In this improved biquad, the sizes of  $C_{IN}$ ,  $C_2$  and  $C_{F2}$  can be drastically reduced because the large time constant is chiefly being realized by the capacitors  $C_1$ ,  $C_3$  and  $C_{F1}$ . This is well illustrated by the transfer function that is written below as

$$H(z) = -\frac{C_{IN}}{C_{F2}} \frac{1 - z^{-1}}{(1 - z^{-1})^2 + (1 - z^{-1}) \frac{C_2}{C_{F2}} + \frac{C_1 C_3 C_4}{C_{F1}^2 C_{F2} \left(1 + \frac{C_1}{C_{F1}}\right)} z^{-1}}. \quad (3.35)$$

The above z-domain transfer function can be converted to s-domain quite trivially as

$$H(s) = - \frac{s \left( \frac{f_{clk} C_{in}}{C_{F2}} \right)}{s^2 + s \frac{f_{clk} C_2}{C_{F2}} + \frac{f_{clk}^2 C_1 C_3 C_4}{C_{F2} C_{F1}^2 \left( 1 + \frac{C_1}{C_{F1}} \right)}}. \quad (3.36)$$

The roots of the denominator will give us the respective corner. Our concern is with the high pass corner. The high pass corner is given by

$$\rho_{HPF} = f_{clk} \frac{C_1 C_3 C_4}{C_2 C_{F1}^2 \left( 1 + \frac{C_1}{C_{F1}} \right)}. \quad (3.37)$$

And the corresponding time constant is given by

$$\tau = \frac{C_2 C_{F1}^2}{C_1 C_3 C_4} \left( 1 + \frac{C_1}{C_{F1}} \right). \quad (3.38)$$

Thus the time constant here is a ratio of three transistors. Thus the loading effect on OTA 2 can be reduced in comparison with the conventional Fleischer-Laker structure. Further, lower spreads can be achieved because now three ratios are involved. The low pass corner is given by

$$\rho_{LPF} = f_{clk} \frac{C_2}{C_{F2}}. \quad (3.39)$$

Both  $C_2$  and  $C_{F2}$  can be small capacitors.

### 3.6.2 Capacitors, matching and sensitivity

If we optimize for spread, Table 3-5 gives the values of the capacitors in numbers of unit capacitors.

Table 3-5: Capacitor values for Fig. 3-14 optimizing spread

Corner	$C_1$	$C_2$	$C_3$	$C_4$	$C_{IN}$	$C_{F1}$	$C_{F2}$
.159 Hz	2	12	2	1	12	28	18
4 Hz	2	4	2	1	4	10	6

Thus, this structure does a better job of reducing spread and area than the Nagaraj integrators. However, for large time constants, OTA 2 might be loaded by  $C_{IN}$ . Thus, we can optimize loading for 0.159 Hz using the values of capacitors as given in Table 3-6.

Table 3-6: Capacitor values for Fig. 3-14 optimizing loading on opa-2

Corner	$C_1$	$C_2$	$C_3$	$C_4$	$C_{IN}$	$C_{F1}$	$C_{F2}$
0.159 Hz	2	2	2	2	2	100	3

Note that if we eliminate  $C_{F2}$ , we get a one-integrator loop with two OTAs. The structure will be a pure high pass. This is not a problem if a stand-alone high pass is required or if the succeeding stage is available to implement a low pass. Thus, we may be able to reduce the area by eliminating  $C_{F2}$ . If we eliminate  $C_{F2}$ , the low pass corner is not defined. It is set by the OTA bandwidth. However, to define the low pass corner, we can have another low pass block following this stage.

The FL biquad using the Nagaraj integrator is more sensitive to capacitor mismatch than the other structures because of the number of capacitor ratios (3) involved in implementing the time constant. The sensitivities are given by

$$\begin{aligned}
 S_{C1}^{HPF} &= S_{C3}^{HPF} = S_{C4}^{HPF} = -1 \\
 S_{C2}^{HPF} &= 1 \\
 S_{CF1}^{HPF} &= 2 \\
 S &= 6.
 \end{aligned} \tag{3.40}$$

### 3.6.3 Op-amp DC gain

If the finite DC gain of the OTA is considered, then again we end up with a zero in the unit circle just as was the case with the conventional Fleisher-Laker biquad. The transfer function is given by

$$H(z) = -\frac{C_{IN}}{C_{F2}(1+A_2^{-1})} \frac{1 - z^{-1} + \frac{C_1}{A_1 C_{F1}}}{(1 - z^{-1})^2 + (1 - z^{-1}) \left( \frac{C_2}{C_{F2}} + \frac{C_1}{A_1 C_{F1}} \right) + z^{-1} \frac{C_1 C_3 C_4}{C_{F1}^2 C_{F2} \left( 1 + \frac{C_1}{C_{F1}} \right)}}. \tag{3.41}$$

Thus the frequency of the zero is given by

$$\rho_z = \frac{f_{clk} C_1}{A_1 C_{F1}}. \tag{3.42}$$

Thus, the DC gain of OTA 1 must be large. Otherwise the zero will be too close to the pole. This is exactly the same as for the conventional Fleischer-Laker biquad.

### 3.6.4 Op-amp GBW

The settling time of OTA 2 is dictated by its  $g_m$  and the parallel combination of  $C_4$ ,  $C_{in}$  and  $C_3$ . The settling of OTA 1 is dictated by its  $g_m$  and  $C_3$  during phase 1 and by  $C_4$  during phase 2. If the large time constant is dictated mainly by the Nagaraj integrator, then settling of the OTA will not be a problem because the  $g_m$  corresponding to minimum power consumption (10nA per transistor) should be enough for all purposes.

### 3.6.5 Op-amp offsets

The output voltage in the presence of op-amp offsets is given by

$$V_{OUT,off} = -\left(1 + \frac{C_{F1}}{C_3}\right)V_{in,off,1}. \quad (3.43)$$

Thus the output offset of the entire biquad is scaled up by the input referred offset of OTA 1, which implements the Nagaraj integrator.

## 3.7 Conclusions

Of the various schemes discussed here, it appears that from the point of view of capacitor area or capacitor spread, the best technique is the one by Nagaraj. All the techniques require identical DC gains and  $g_m$  from the OTA for implementing the same time constant. Thus, it is the Nagaraj technique, which will be compared with the high pass structures that we will present in the next chapter.



## CHAPTER IV

### LARGE TIME CONSTANTS IN SC HIGH PASS FILTERS

This chapter includes the main contributions of this thesis. To the author's knowledge, no work on achieving large time constants in switched-capacitor high pass filters or differentiators has ever been reported in literature. All the structures in this chapter are thus the contributions of this thesis. As was pointed out in the first chapter, the main motivation for focusing on SC HPFs is that they are the most natural way to implement low frequency high pass corners in wideband applications. Another advantage is that they conserve power. A conventional method of implementing a high pass function is by subtracting a low pass function from a unity gain buffer, i.e.  $HPF = 1 - LPF$ . Thus, if we could realize a high pass structure as is, we could eliminate the buffer. We begin with a discussion on differentiators and then move on to high-pass filters.

#### 4.1 Realizing a Differentiator

A conventional switched-capacitor differentiator is shown in Fig. 4-1.

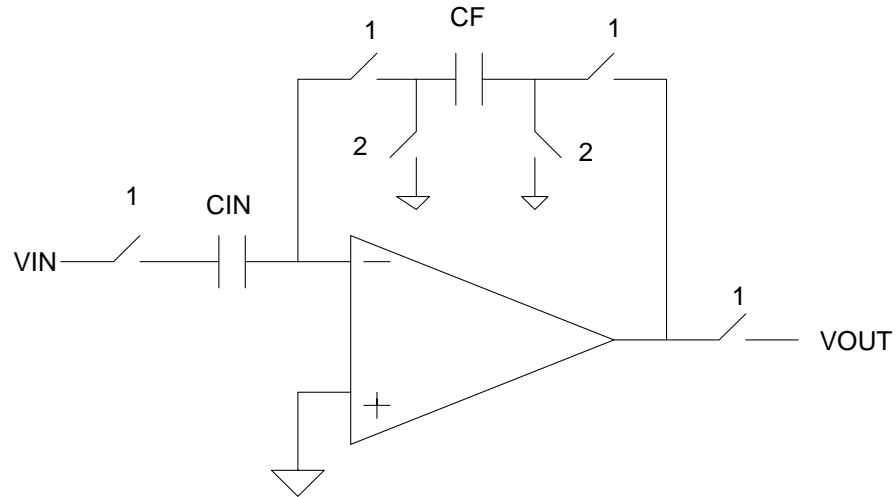


Fig. 4-1: Conventional SC differentiator

The ideal z-domain transfer function is given by

$$H(z) = -\frac{C_{IN}}{C_F}(1 - z^{-1}). \quad (4.1)$$

For slowly carrying input signals, large time constants are required. The time constant is given by

$$\tau = T_{CLK} \frac{C_{IN}}{C_F}. \quad (4.2)$$

$T_{CLK}$  is the clock frequency. For very large time constants,  $C_{IN}$  could occupy a very large on-chip area.

## 4.2 Basic High Pass Filter

The basic continuous-time HPF is given below in Fig. 4.2.

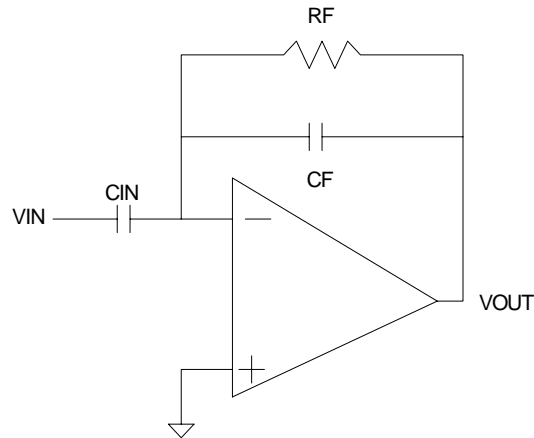


Fig. 4-2: Conventional continuous time high pass filter

To have a large time constant  $C_F$  and  $R_F$  must both be made as large as possible. However, to maintain the passband gain  $C_{IN}$  must also be scaled up along with  $C_F$ . Thus for large time constants all the components must be increased. The discrete-time version of the SC HPF is shown in Fig. 4-3.

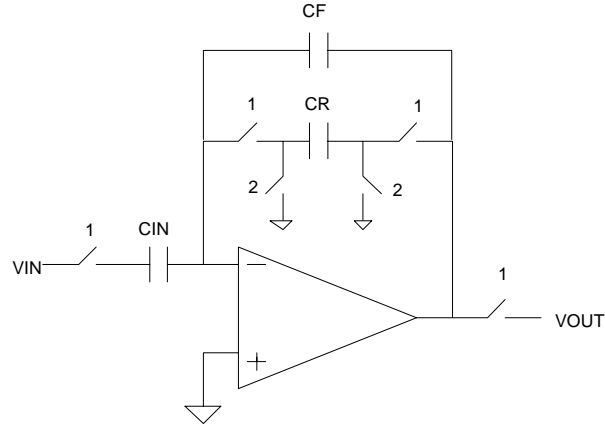


Fig. 4-3: Conventional SC high pass filter

The z-domain transfer function is given by

$$H(z) = -\frac{C_{IN}}{C_F} \frac{1 - z^{-1}}{1 - z^{-1} + \frac{C_R}{C_F}}. \quad (4.4)$$

The time constant is given by

$$\tau = \frac{1}{f_{clk}} \frac{C_F}{C_R}. \quad (4.5)$$

And the gain is given by  $C_{IN}/C_2$ . Thus, for large time constants  $C_R$  must be made small while  $C_F$  must be made large. To maintain gain,  $C_{IN}$  must also be scaled up with  $C_F$ . However, scaling up  $C_{IN}$  and  $C_F$  requires amplification circuitry, which cannot be implemented using passive components. Besides, scaling up  $C_{IN}$  will place a severe stress on the settling time of the OTA during phase 1, which is the high-pass filtering phase (phase 2 is the reset phase for  $C_R$  and the idle phase for the OTA). This is readily apparent by breaking the OTA feedback loop at the inverting terminal during phase 1 as shown in Fig. 4-4.

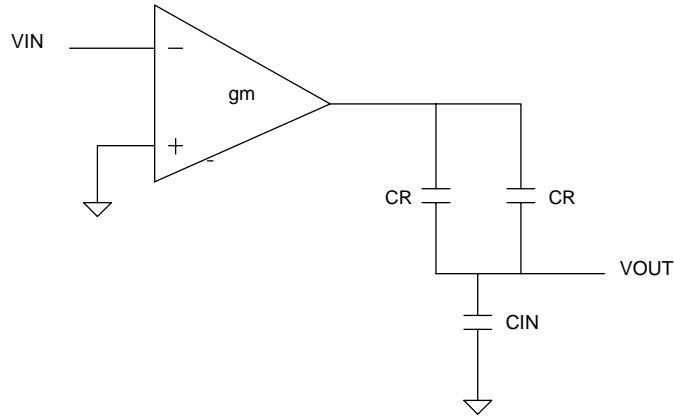


Fig. 4-4: Illustrating loading by breaking the feedback loop in Fig. 4-3

The loop gain of the overloaded circuit is given by

$$\frac{V_{out}}{V_{in}} = \frac{g_m}{sC_{IN}}. \quad (4.5)$$

And the GBW of the loop gain is given by

$$f_{GBW} = \frac{g_m}{2\pi C_{IN}}. \quad (4.6)$$

Thus we need a larger  $g_m$  as the  $C_{IN}$  increases. And a larger  $g_m$  is obtained only by increasing the power consumption of the OTA.

A second solution to large time constants involves the reduction of  $C_R$ . Thus we will concentrate on techniques to reduce the effective size of  $C_R$ .

### 4.3 Partial Positive Feedback

The basic idea of partial positive feedback is given for a continuous time high pass filter below in Fig. 4-5.

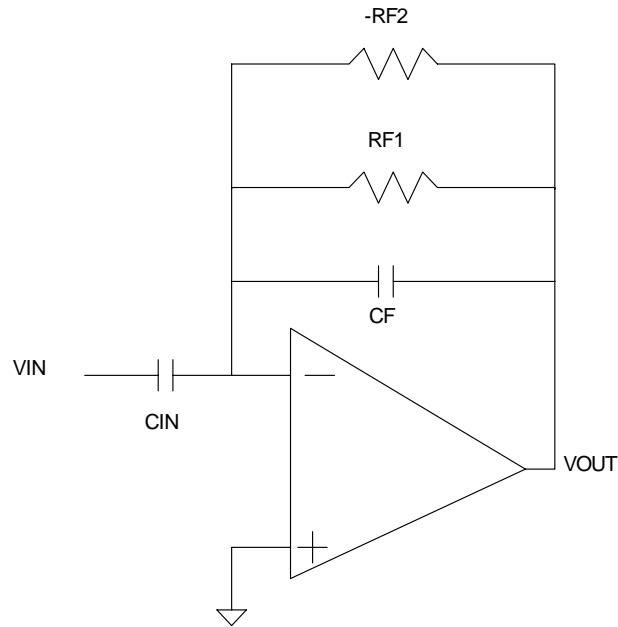


Fig. 4-5: Conceptual partial positive feedback (conductance subtraction)

A positive resistance is placed in parallel with a negative resistance. The positive resistance is slightly less than the negative resistance (positive conductance is slightly greater than the negative conductance). Thus the parallel combination would yield a positive resistance that is quite large (or a positive conductance that is quite small). The switched-capacitor implementation of just such an idea is shown below in Fig. 4-6.

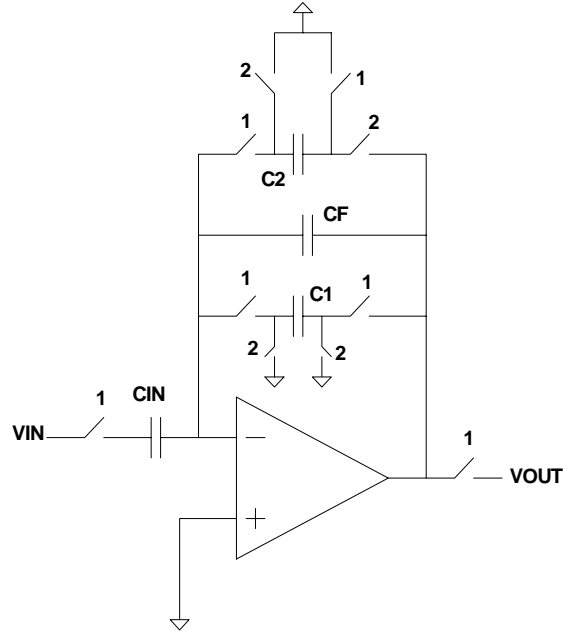


Fig. 4-6: Simple SC implementation of partial positive feedback

The z-domain transfer function is given by

$$\frac{V_{OUT}(z)}{V_{IN}(z)} = -\frac{C_{IN}}{C_F + C_2} \frac{1 - z^{-1}}{1 - z^{-1} + \frac{C_1 - C_2}{C_F + C_2}}. \quad (4.7)$$

And the time constant being implemented is given by

$$\tau = \frac{1}{f_{clk}} \frac{C_F + C_2}{C_1 - C_2}. \quad (4.8)$$

Thus, for a large time constant  $C_1$  should be slightly greater than  $C_2$ . However, *as in any scheme involving partial positive feedback, the sensitivity of the time constant increases as the difference between  $C_1$  and  $C_2$  is lowered.*  $C_1$  and  $C_2$  cannot be made arbitrarily close to each other. The circuit depends on the closeness of  $C_1$  and  $C_2$  and not

on the ratio. Thus it is not possible to match  $C_1$  and  $C_2$  to arbitrarily close values using *unit capacitors*.

A more sophisticated structure using partial positive feedback, but allowing the use of unit capacitors for better matching is given below in Fig. 4-7.

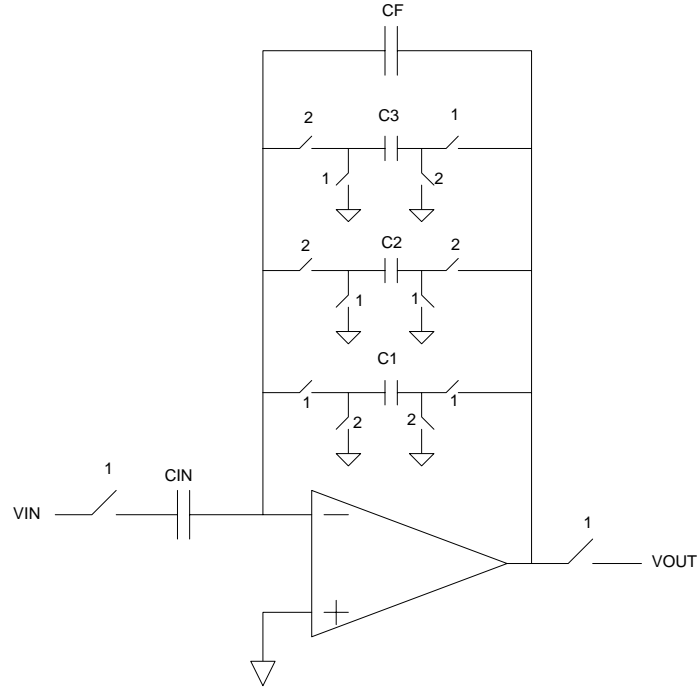


Fig. 4-7: A sophisticated SC implementation of partial positive feedback

The z-domain transfer function of this structure is given by

$$H(z) = \frac{C_{IN}}{C_F + C_1} \frac{1 - z^{-1}}{1 - z^{-1} + z^{-1} \frac{C_1 C_3 + C_F (C_1 + C_3 - C_2)}{(C_F + C_1)(C_F + C_3)}}. \quad (4.9)$$



And the time constant is given by

$$\tau = \frac{1}{f_{clk}} \frac{(C_F + C_1)(C_F + C_3)}{C_1 C_3 + C_F (C_1 + C_3 - C_2)}. \quad (4.10)$$

If  $C_1=C_3=C$  and  $C_2=2C$  and  $C_F=C_{IN}=\beta C$ , then theoretically very large time constants can be obtained since the time constant changes to

$$\tau = \frac{(\beta + 1)^2}{f_{clk}}. \quad (4.11)$$

$\beta$  is the capacitor ratio. However, note that this technique relies on the assumption that the sum of  $C_1$  and  $C_3$  can be made equal to  $C_2$ . Thus this structure is very sensitive to variations in  $C_1$ ,  $C_2$  and  $C_3$ . To demonstrate this sensitivity, let  $C_1=C_3=C$  and  $C_2=2(C+\Delta C)$  and  $C_F=C_{IN}=\beta C$ . The time constant in this presence of this mismatch on the part of  $C_2$  is given by

$$\tau = \frac{(\beta + 1)^2}{f_{clk} \left( 1 + \beta \frac{\Delta C}{C} \right)}. \quad (4.12)$$

The sensitivity of the time constant with respect to the capacitor ratio mismatch is approximately given by

$$S_{\frac{\Delta C}{C}}^{\tau} \approx \beta. \quad (4.13)$$

Thus, the sensitivity increases with the capacitor ratio. As an example, consider that a high pass corner of 1Hz requires a capacitor ratio of 20. A 0.5% mismatch in capacitor ratio can thus cause a 10% error in the time constant. Therefore this method is more suitable for medium time constants (which require smaller capacitor ratios), not for large ones (larger ratios).

#### 4.4 Attenuated Feedback HPF

Partial positive feedback causes the circuit to be too sensitive to process variations since it relies on capacitive cancellation and not capacitive ratios. However, the technique of attenuated feedback relies on ratios and, as a rule the resulting structure should be much less sensitive to process variations.

The basic idea of attenuated feedback in continuous time HPF is illustrated in Fig. 4-8.

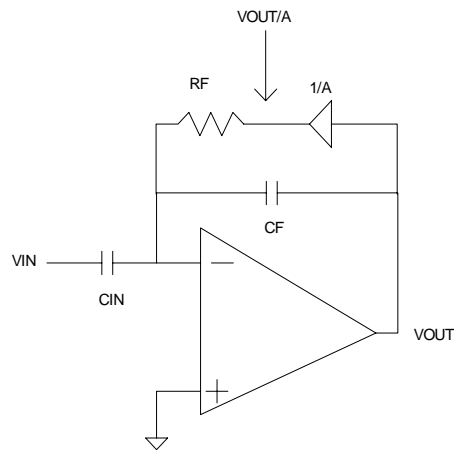


Fig. 4-8: Conceptual attenuated feedback

By attenuating the output, the resistor looks much larger than it actually is. By simulating a larger resistance, we can obtain a larger time constant. In a switched-capacitor circuit, a larger resistance means a smaller capacitor. The idea for a switched-capacitor is illustrated in Fig. 4-9.

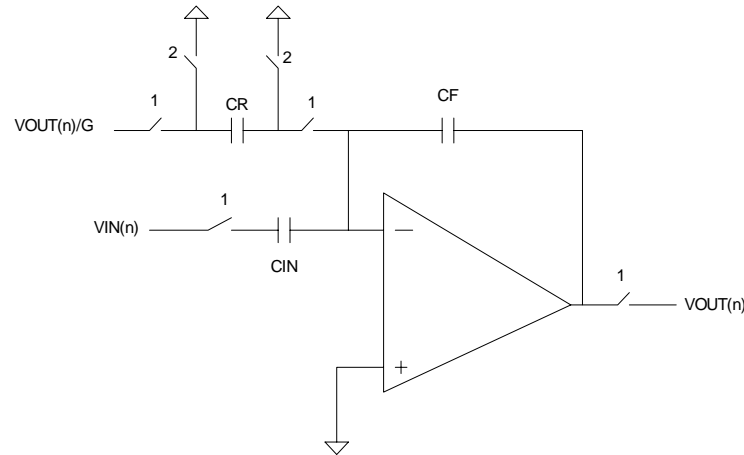


Fig. 4-9: Conceptual SC implementation of attenuated feedback

Notice in Fig. 4-9 that  $V_{OUT(n)}$  and  $V_{OUT(n)}/G$  (the attenuated version of the output) are available at the same instant. In switched-capacitor circuits, this is not possible. Thus, we somehow have to make do with an attenuated version of the output from the previous phase (or previous sample). To prevent positive feedback, we need  $-V_{OUT(n-1)}/G$  when the input  $V_{IN(n)}$  is being sampled. One way to do this using the T-Cell technique is shown below in Fig. 4-10.

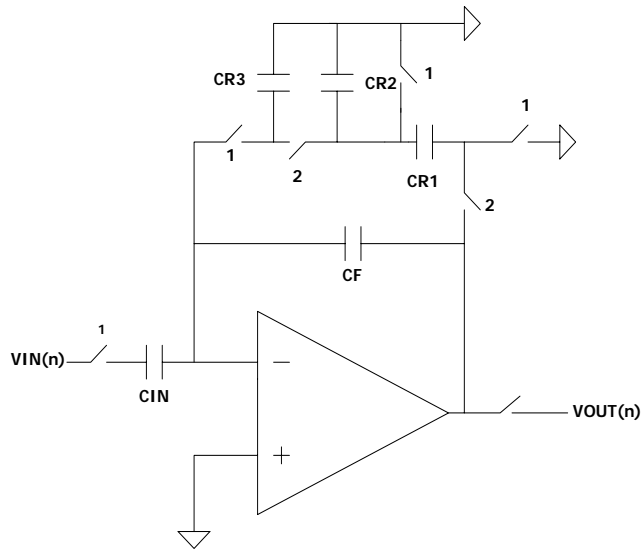


Fig. 4-10: The T-Cell technique adapted to high pass filters

In the above structure  $C_{IN}=C_F=C_{R2}=BC_{R1}$ . The time constant can be shown to be

$$\tau = \frac{(\beta + 1)^2}{f_{clk}}. \quad (4.14)$$

However, the obvious problem is that this structure is not parasitic-insensitive.

Thus some other way to attenuate the feedback must be found.

One very obvious way to attenuate the feedback using an extra OTA is given below in Fig. 4-11.

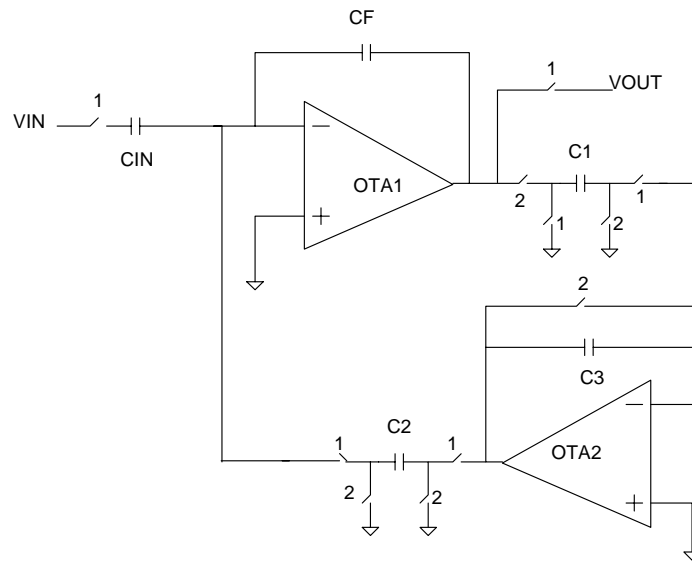


Fig. 4-11: Attenuated feedback in SC HPFs using two OTAs

However, this method uses an extra-OTA, just the problem we were trying to avoid while using the low pass filter. In Fig. 4-11, OTA 2 performs the attenuation. An obvious question arises. Can we use OTA 1 itself to perform the attenuation during phase 2? The answer in single ended structure is no. The reason is that any such attempt to attenuate the output and feed back the charge to the non-inverting terminal during the next phase will lead to positive feedback. That is because OTA 1 cannot generate the attenuated sample of the correct polarity in the one phase that is available. However, in fully differential circuits, this problem is solved, as outputs of both polarities are available. The switched-capacitor implementation of this new HPF is shown below in Fig. 4-12.

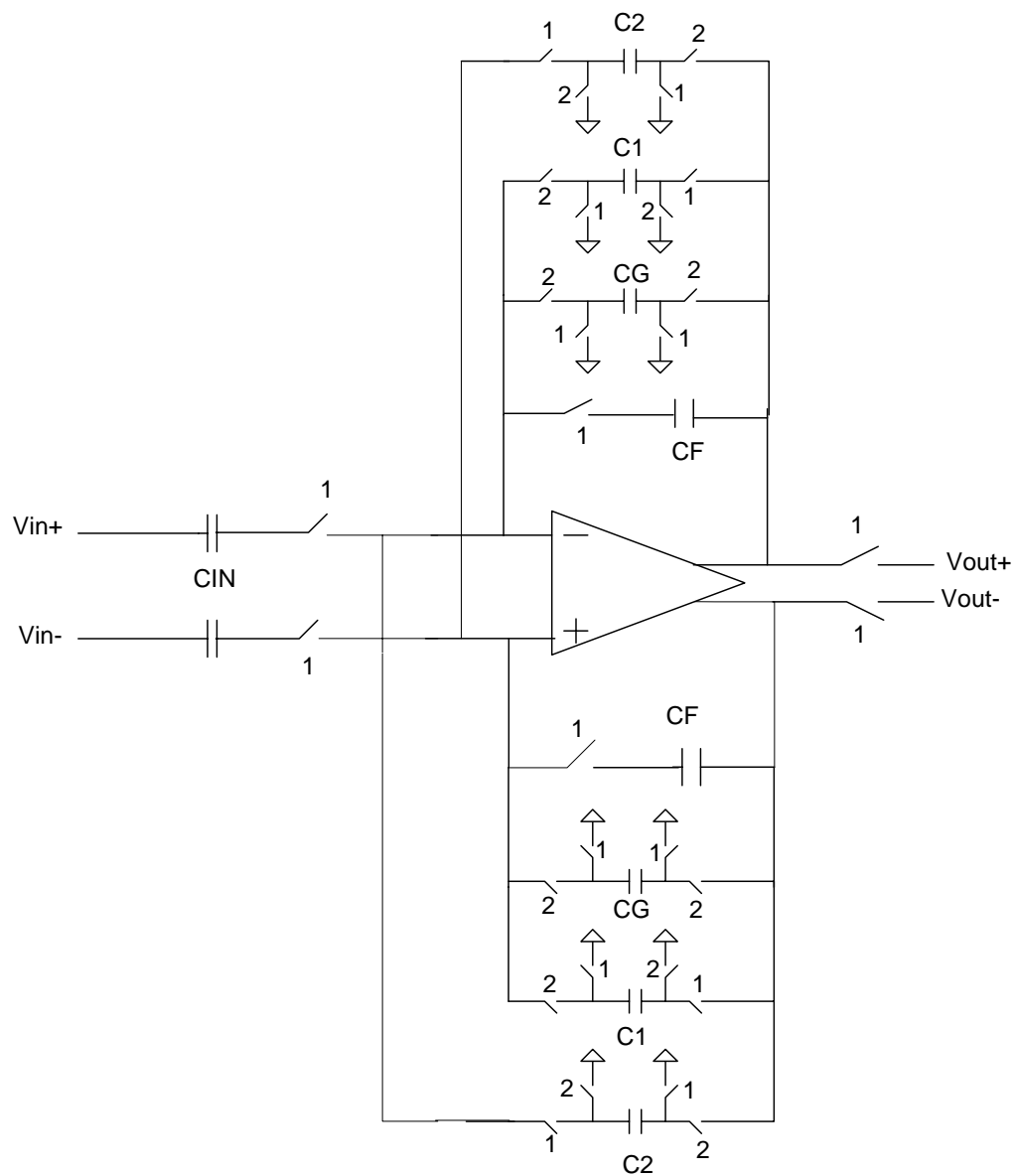


Fig. 4-12: Fully differential LTC SC HPF using only one OTA

In the structure above the attenuation is achieved by  $C_1$  and  $C_G$  and is given by  $C_1/C_G$ . That attenuated voltage is stored on  $C_2$ . This is illustrated in Fig. 4-13a.

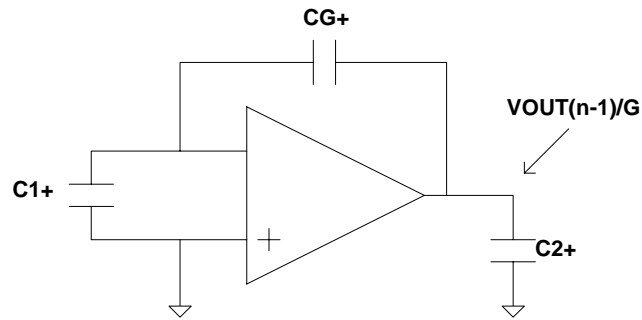


Fig. 4-13a: HPF of Fig. 4-12 in phase 2 performing attenuation

During phase 1, the voltage stored on  $C_2$  from phase 2 is used for the high pass filtering. Fig. 4-13b illustrates exactly what is happening during phase 2.

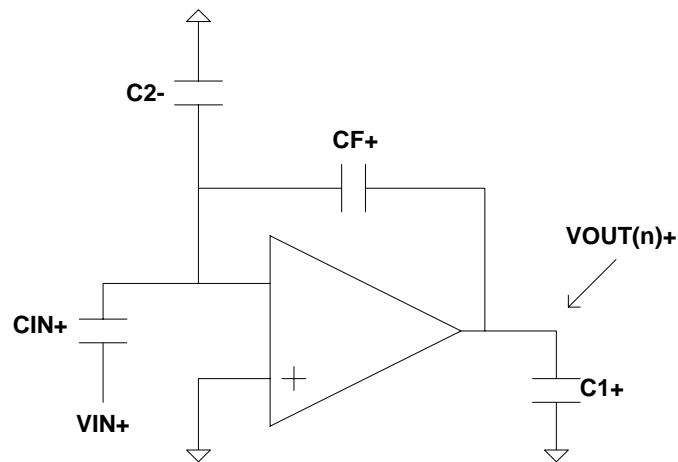


Fig. 4-13b: HPF of Fig. 4-12 in phase 1 performing high pass filtering

Note that because of the nature of the feedback, this structure has no single ended equivalent. The transfer function of the structure above is given by

$$H(z) = \frac{C_{IN}}{C_F} \frac{1 - z^{-1}}{1 - z^{-1} + \frac{C_1 C_2}{C_G C_F}}. \quad (4.15)$$

The time constant is given by

$$\tau = \frac{C_G C_F}{C_1 C_2} \frac{1}{f_{clk}}. \quad (4.16)$$

For large time constants,  $C_G$  and  $C_F$  should be larger than  $C_1$  and  $C_2$ . If  $C_{IN} = C_F = C_G = \beta C$ ,  $C_1 = C_2 = C$ , then the time constant is given by  $\tau = \beta^2 / f_{clk}$ .

#### 4.4.2 Capacitors, matching and sensitivity

From Fig. 4-13a and Fig. 4-13b, capacitors  $C_{IN}$ ,  $C_2$  and  $C_F$  form one cluster. Capacitors  $C_G$  and  $C_1$  form the other cluster. The capacitor values are given in Table 4-1.

Table 4-1: Capacitor values for Fig. 4-12

Corner (Hz)	$C_1$	$C_2$	$C_{IN}$	$C_F$	$C_G$
4 Hz	1	1	10	10	10
0.159 Hz	1	1	50	50	50

The sensitivities all capacitor ratios with respect to the time constant have a magnitude of 1. This is the same as for the Nagaraj technique and the conventional Fleischer-Laker biquad and less than the FL-Nagaraj implementation.



#### 4.4.3 Op-amp DC gain

If the op-amp DC gain is considered, then the transfer function can be written as

$$H(z) = \frac{C_{IN}}{C_F \left( 1 - \frac{C_1 C_2}{A C_G C_F} \right)} \frac{1 - z^{-1}}{1 - z^{-1} + \frac{C_2}{A C_F} + \frac{C_1 C_2}{C_G C_F}}. \quad (4.17)$$

The corner frequency is given by

$$\rho = f_{clk} \left( \frac{C_1 C_2}{C_G C_F} + \frac{C_2}{A C_F} \right). \quad (4.18)$$

The error in time constant is thus given by

$$\varepsilon = \frac{C_G}{A C_1} = \frac{\beta}{A}. \quad (4.19)$$

Thus, as the time constant increases (corner frequency decreases), the DC gain requirements also increase. For a corner of 0.159 Hz and a clock of 2.5 KHz, a DC gain of 5000 (74dB) is required for an error requirement of 1%.

#### 4.4.4 Op-amp GBW

This feature is the main disadvantage of high pass filters with respect to low pass filters. The critical phase for loading is phase 1. During phase 1, the OTA is loaded by  $C_{IN}$ , which is as large as  $C_F$  or  $C_G$ . The loading diagram is illustrated in Fig. 4-14. The circuit on the left shows the equivalent closed loop representation during phase 2. The circuit on

the right shows the open loop representation by breaking the feedback loop and injecting a test signal ( $V_{IN}$ ).

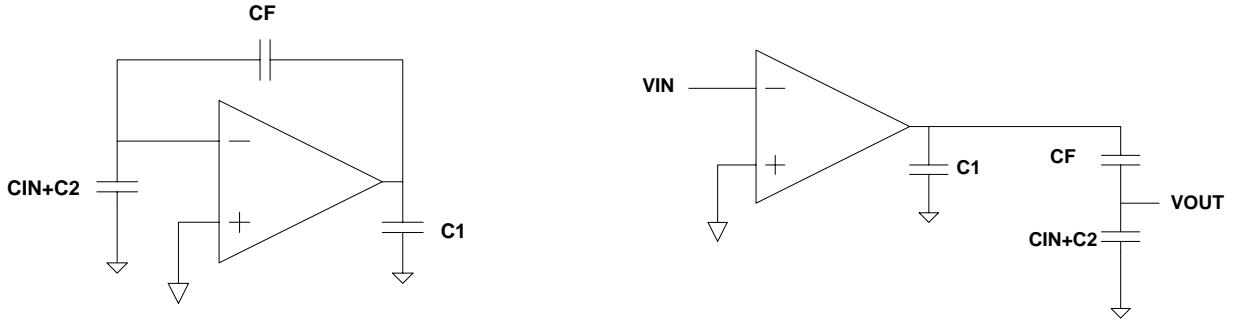


Fig. 4-14: Loading on OTA of Fig. 4-12 during phase 1

The loop GBW is given by

$$loop\_GBW = \frac{g_m}{C_{IN} + C_2 + C_1 \left( 1 + \frac{C_{IN} + C_2}{C_F} \right)}. \quad (4.20)$$

As the time constants get larger  $C_{IN}$  gets larger. This increases the required  $g_m$  of the OTA. For medium-large time constants,  $g_m$  is not a problem because the minimum  $g_m$  (power consumption) is set by other considerations mentioned in Chapter 2. However, as the time constants get larger, so does  $C_{IN}$  and the loading on the OTA becomes very large.

Finally, there is one more strain on the GBW. This structure requires more than 5 time constants for the output voltage to settle within the required accuracy of 1%. Note that the OTA in Fig. 4-12 swings by very large amounts between the two clock phases.

The reason is that in one phase, the output is attenuated (to a small value) and in the next phase, it is again a large value. This is illustrated in Fig. 4-15.

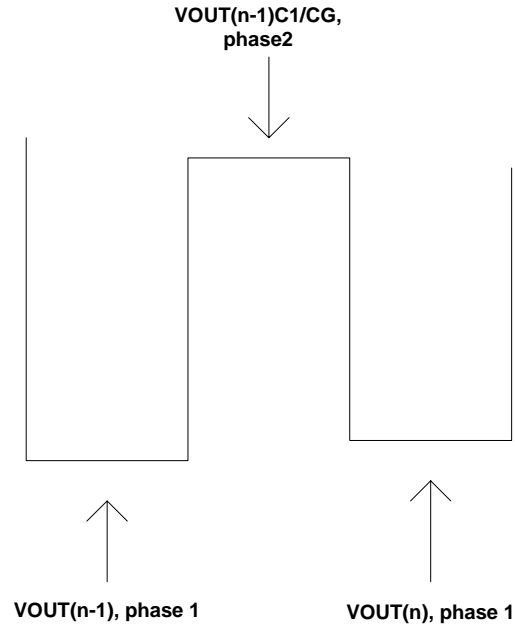


Fig. 4-15: Transient waveforms for the structure of Fig. 4-12

In any SC filtering application, the quantity of importance is  $V_{OUT(n)} - V_{OUT(n-1)}$ . Thus, this difference must settle to within 1% for 1% accuracy. Thus the number of time constants required to settle can be derived to be

$$N_T = 5 + \ln\left(\frac{C_F C_G}{C_1 C_2}\right). \quad (4.21)$$

Thus, as the time constant increases, not only does the loading increase, but the number of time constants required to settle to the required accuracy also increases.

#### 4.4.5 Op-amp offsets

Just like in the Nagaraj technique, the input referred offset of this structure appears at the output magnified by a factor of  $C_G/C_1$ , which is the attenuation factor. This can be intuitively understood by considering that a large attenuating factor means the transportation of very small amounts of charges via small voltage differentials. For large time constants, these voltages become comparable to the input referred offsets, which appear at the output amplified by the attenuation factor.

### 4.5 Differentiators

The technique above can also be adapted to provide differentiators having very large time constants. Differentiators are required in some biomedical or electrochemical applications [2-3], where continuous time processing of an analog signal is required. Other applications include use in audio equalizers. Fig. 4-16 illustrates a differentiator using the technique previously discussed.

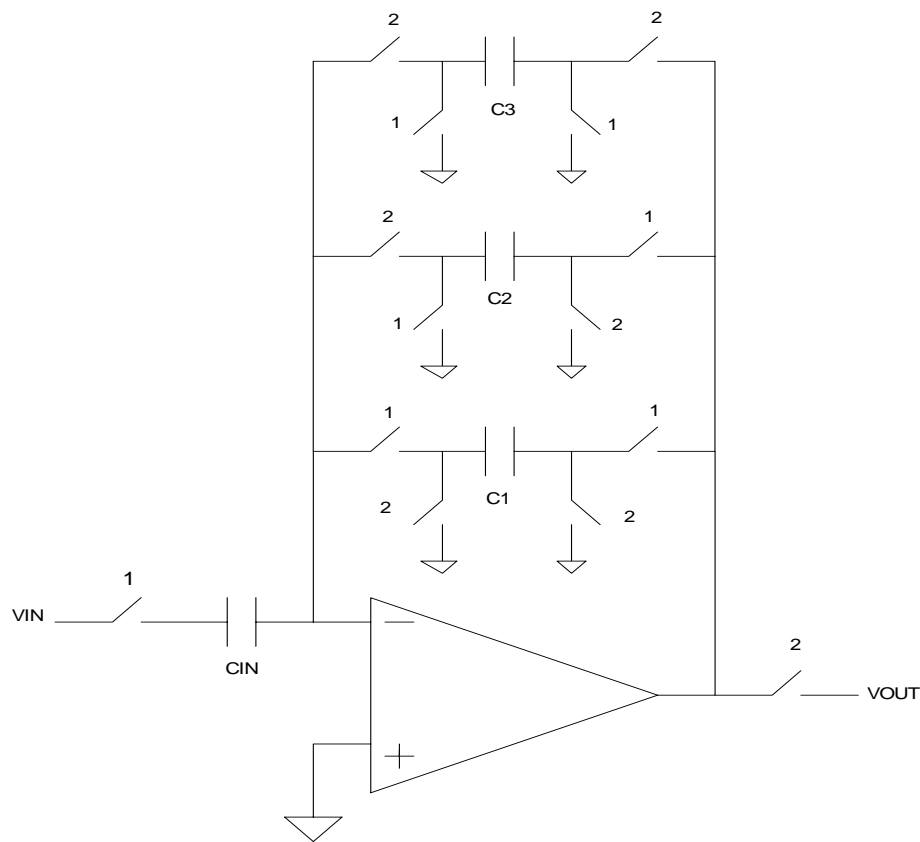


Fig. 4-16: Large time constant SC differentiator

The z-domain transfer function can be expressed as

$$H(z) = -\frac{C_2 C_{IN}}{C_1 C_3} (1 - z^{-1}) z^{-1/2}. \quad (4.22)$$

The time constant is given by

$$\tau = \frac{C_2 C_{IN}}{C_1 C_3}. \quad (4.23)$$

## 4.6 Noise Analysis

Unfortunately, Cadence Spectre does not have the ability to perform noise analysis of switched-capacitor circuits. However, a bit of insight is necessary in order to understand the noise issues and tradeoffs involved. One way to acquire such insight is to analyze the continuous time counterparts of these switched-capacitor circuits. While not very accurate, they provide us with some degree of insight in comparing the various topologies. In the following subsections, we will perform the noise analysis of the FL biquad, the Nagaraj LPF and the proposed HPF.

### 4.6.1. Proposed HPF

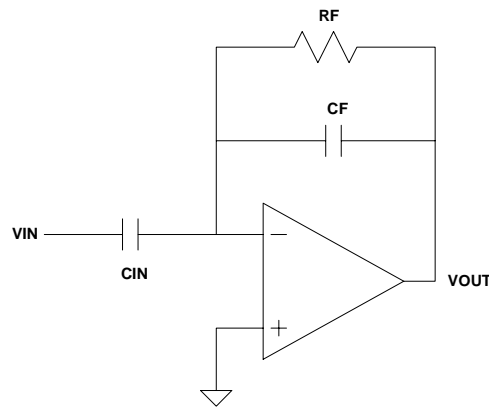


Fig. 4-17a: The CT HPF

Fig. 4-17a is used as a reference to compute the noise of the proposed HPF. The total noise originating from  $R_F$  is given by

$$v_{n,out}^2 = \frac{kT}{C_F}. \quad (4.24)$$

The noise spectral density from the OTA is given by

$$v_{n,out}^2(s = j2\pi f) = \frac{4KT\gamma}{g_m} \left| 1 + \frac{sR_F C_{IN}}{1 + sR_F C_F} \right|^2. \quad (4.25)$$

$g_m$  is the trans conductance of the OTA. The output referred noise decreases with large time constants. The effect of  $C_{IN}$  does not appear in the equation. However, in real SC circuits, a large  $C_{IN}$  reduces the noise of the switches and also the noise of the OTA in the previous stage. Flicker noise has not been considered as it is assumed to be chopped out of band by the chopper clock. Let us just compute the total noise for the two cases of a 0.159Hz HP corner and a 4Hz HP Corner. For a 0.159HZ Corner,  $R_F C_F = 1 = R_F C_{IN}$ . Further  $C_F = C_{IN} = 12.5\text{pF}$ .  $g_m = 0.3\text{uA/V}$ . For a detailed derivation of these values, the reader is urged to jump to section 5.2 in Chapter V. We are using these values simply to get a pulse on the noise in the circuit. The integrated noise from the resistor is calculated as

$$v_{n,outR}^2 = \frac{kT}{C_F} = \frac{4 \times 10^{-21}}{12.5 \times 10^{-12}} = 3.2 \times 10^{-10} \text{V}^2. \quad (4.26)$$

The noise from the OTA will have to be integrated in the bandwidth from 0.159Hz to 200Hz. The mathematical derivation proceeds as

$$v_{n,out,OTA}^2 = \frac{4kT\gamma}{g_m} \int_{0.159}^{200} \left| \frac{1 + j4\pi f R_F C_{IN}}{1 + j2\pi f R_F C_F} \right|^2 df = 2.56 \times 10^{-11} \text{V}^2. \quad (4.27)$$

Thus the total output noise can be given by  $3.456 \times 10^{-10} \text{V}^2$  for a cutoff of 0.159Hz. For a cutoff frequency of 4Hz, the total thermal noise power would be  $1.6 \times 10^{-9} \text{V}^2$ .

#### 4.6.2. Nagaraj LPF

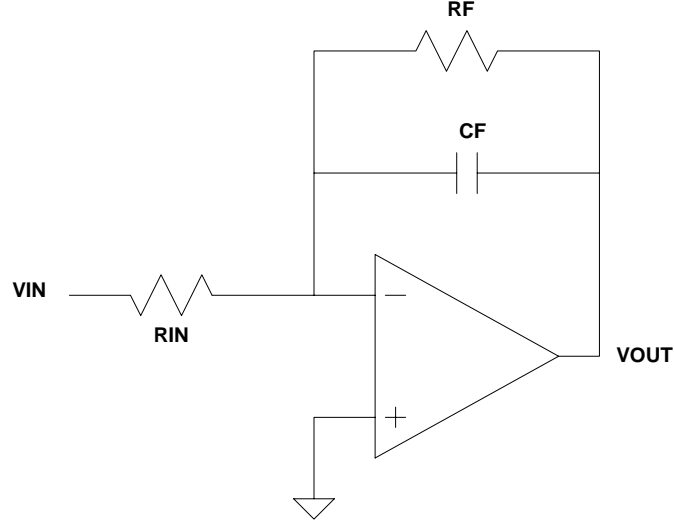


Fig. 4-17b: The CT LPF

Fig. 4-17b is used a reference to compute the noise of the Nagaraj LPF. The noise spectral density of the  $g_m$  stage is given by

$$v_{n,out}^2 = \frac{4kT\gamma}{g_m} \left( 1 + \frac{R_F}{R_{IN}} \frac{1}{1 + j2\pi f C_F R_F} \right)^2. \quad (4.28)$$

For 0.159Hz,  $R_F C_F = 1$ ,  $C_F = 24.5\text{pF}$  and for 4Hz,  $R_F C_F = 1/25$ ,  $C_F = 4.5\text{pF}$ .

$g_m = 0.25\text{uA/V}$  for each of these cases. The derivation of all these values is shown in section 5.3 in Chapter V. For each of these cases, we could integrate the noise in the bandwidth to obtain

$$\begin{aligned} (v_{n,out}^2)_{0.159\text{Hz}} &= 10^{-11} \text{V}^2 \\ (v_{n,out}^2)_{4\text{Hz}} &= 1.3 \times 10^{-11} \text{V}^2 \end{aligned} \quad (4.29)$$



The noise spectral density due to  $R_F$  and  $R_{IN}$  is given by

$$\begin{aligned} (v_{n,R}^2)_{0.159Hz} &= \frac{2kT}{C_F} = 3.2 \times 10^{-10} V^2 \\ (v_{n,R}^2)_{0.159Hz} &= 1.6 \times 10^{-9} V^2. \end{aligned} \quad (4.30)$$

However, to implement a high pass corner, two more buffers are needed as shown in Fig. 4-17c.

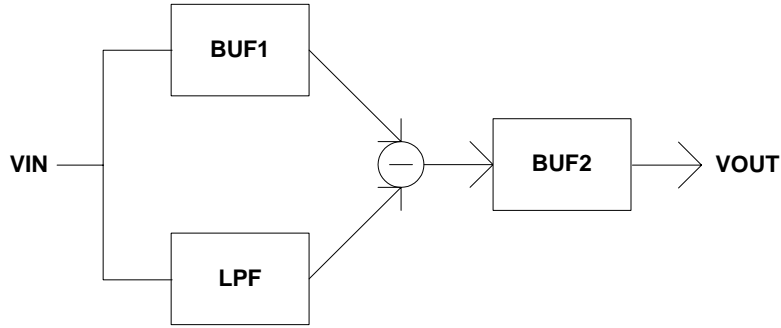


Fig. 4-17c: HPF implementation using buffers and an LPF

The two buffers add extra noise of their own. The noise from the buffers is given by

$$v_{n,out}^2 = \frac{5kT}{C_{BUF1}} + \frac{9kT}{C_{BUF2}} + \frac{16kTB\gamma}{g_{m,buf1}} + \frac{9kTB\gamma}{g_{m,buf2}}. \quad (4.31)$$

$B$  denotes the bandwidth in which the noise is integrated and  $C_{BUF}$  denotes the value of the cap used in the buffer. This noise hardly changes with changes in the time constant. Indeed, the noise from the buffers is the dominant source of noise in this implementation. Even assuming that the Buffer capacitors are equal to the feedback capacitor in the LPF (unrealistic), it is clear that this noise is dominant. If we assume that the buffer capacitors equal 5pF each, the total noise would be  $1.1e-8V^2$ , which is much

higher than the HPF noise. Thus using extra buffers to realize a high pass function using a LPF not leads to greater power consumption, but also greater noise.

#### 4.6.3. FL biquad

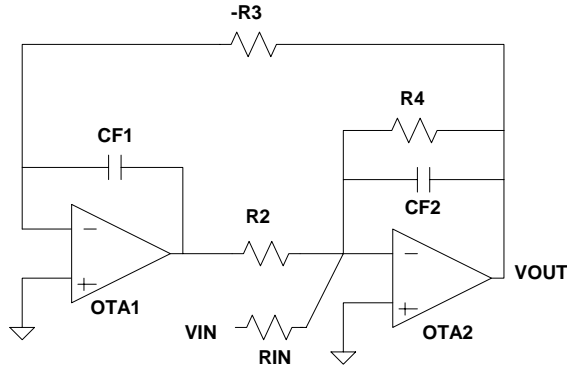


Fig. 4-17d: CT FL biquad

Fig. 4-17d will be used as a reference to compute the noise of the FL-Nagaraj structure.

The noise of the FL biquad is given by

$$v_{n,out}^2 = \frac{kT}{C_{F2}} \left( 1 + \frac{R_4}{R_{IN}} \right) + v_{n,OTA1}^2 \left( \frac{\left( 1 + \frac{1}{sC_3R_3} \right) \left( \frac{R_4}{R_2} \frac{1}{1 + sC_4R_4} \right)}{1 + loop\_gain} \right)^2 + G v_{n,OTA2}^2$$

$$G = \frac{\left( 1 + \frac{R_4}{R_2 \parallel R_{IN}} \frac{1}{1 + sC_{F2}R_4} \right)^2}{(1 + loop\_gain)^2} .$$

(4.32)

Above,  $loop\_gain$  denotes the gain of the 2-integrator loop. The loop gain is given by

$$loop\_gain = -\frac{1}{sR_3C_{F1}} \left( 1 + \frac{R_4}{R_2} \frac{1}{1 + sR_4C_{F2}} \right). \quad (4.33)$$

Note that the loop gain at DC is very large. Thus the FL biquad effectively suppresses the 1/f noise and the offsets of the OTA. This feature is not available in first order structures discussed in sections 4.6.1 and 4.6.2. We will perform the noise analysis for the cases where total spread is minimized. The reason is that so far whenever we have compared topologies, we did it while optimizing spread in all cases. Therefore, we will use the values in Table 3-5, with the unit capacitor equal to 0.25pF. The dominant noise in the equation above comes from the thermal noise of  $R_{IN}$  and  $R_4$ . The total noise is

$$\begin{aligned} (v_n^2)_{0.159Hz} &> 1.78 \times 10^{-9} V^2 \\ (v_n^2)_{4Hz} &> 5.3 \times 10^{-9} V^2. \end{aligned} \quad (4.34)$$

Thus the noise in the biquad is intermediate between the proposed topology and the Nagaraj low pass.

#### 4.6.4 Conclusions of noise analysis

From the noise analysis performed, two things are immediately apparent:

1. The FL biquad suppresses Flicker noise unlike first order structures.
2. The noise of the LPF is the greatest and this comes from the buffers
3. Noise reduces with larger time constants because the capacitor areas increase.
4. The proposed HPF has the lowest noise.

From calculations, it becomes apparent that the proposed HPF has the best noise performance when it comes to thermal noise.

#### 4.7 Comparisons

Tables 4-2 and 4-3 compare various topologies. The two tables show the comparisons for different 3-dB corner frequencies.

Table 4-2: Table of comparisons for various structures for a 4Hz 3-dB corner

Topology	Cap ratio	Cap area	OTA gain	Sensitivity	Power
Std. FL	10	66 units	74 dB	4	60nA
Split-I	4	44 units	74 dB	6	60nA
Nagaraj LPF	9	68 units	60 dB	4	80nA
FL-Nagaraj	5	34 units	74 dB	6	60nA
Proposed HPF	10	64 units	60 dB	4	40 nA

Table 4-3: Comparison table for various structures for a 0.159 Hz 3 dB corner

Topology	Cap ratio	Cap area	OTA gain	Power
Std. FL	50	306 units	74 dB	60nA
Split-I	14	204 units	74 dB	60nA
Nagaraj LPF	49	228 units	74 dB	80nA
FL-Nagaraj	14	120 units	74 dB	60nA
Proposed HPF	50	304 units	74 dB	90 nA

Of these, we will now consider only three structures because these will be the ones that will be compared in the pre-amp design of the following chapter. The three structures are:

1. The proposed HPF
2. The Nagaraj LPF
3. The FL-Nagaraj biquad

The plots of Figs. 4-18, 4-19 and 4-20 compare the three structures for the parameters of power, area and noise.

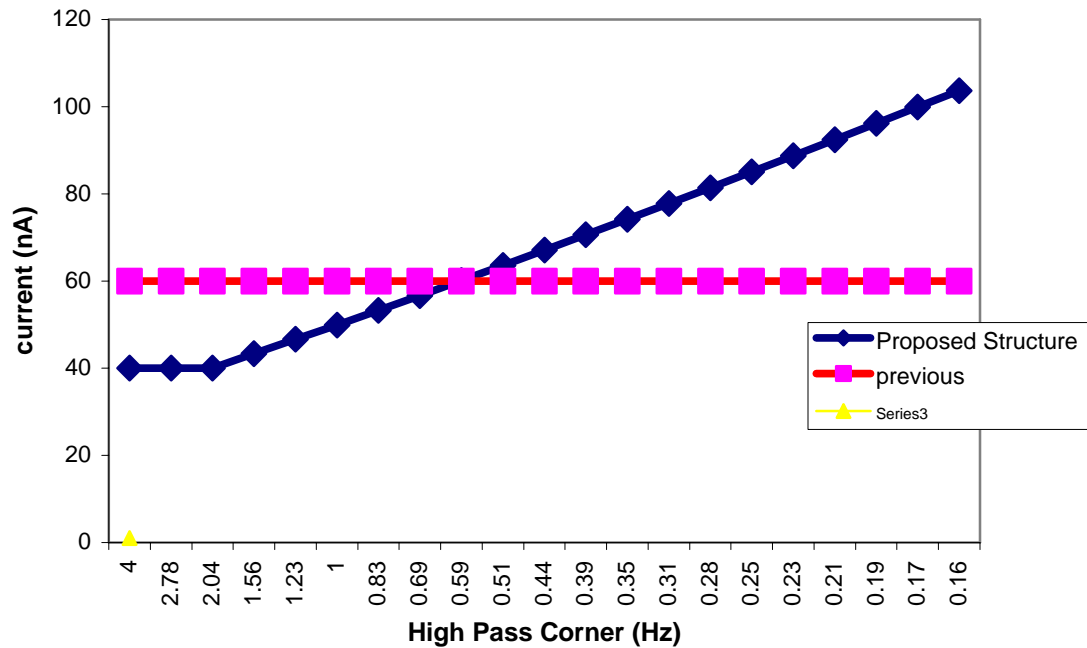


Fig. 4-18: Power comparison plots

Fig. 4-18 shows the power comparison plots. For small to medium time constants, the power consumption is set by constraints other than the required GBW and DC gain (see Chapter II). For such frequencies, the proposed HPF saves power because it uses only one OTA as compared to two for the others. For smaller HP corners, the power consumption of the HPF increases because the size of the input capacitor rises. For the other two structures, the size of the input capacitor remains the same and only the size of the feedback capacitor rises. Thus larger time constants have no effect on the power consumption of the Nagaraj LPF or the FL-Nagaraj structure. In fact, the plots of

power consumption of the Nagaraj LPF and the FL-Nagaraj biquad are superimposed on each other. Thus, there appear to be only two plots when there are actually three. The cross over frequency where the power consumption of all structures is the same is 0.6Hz.

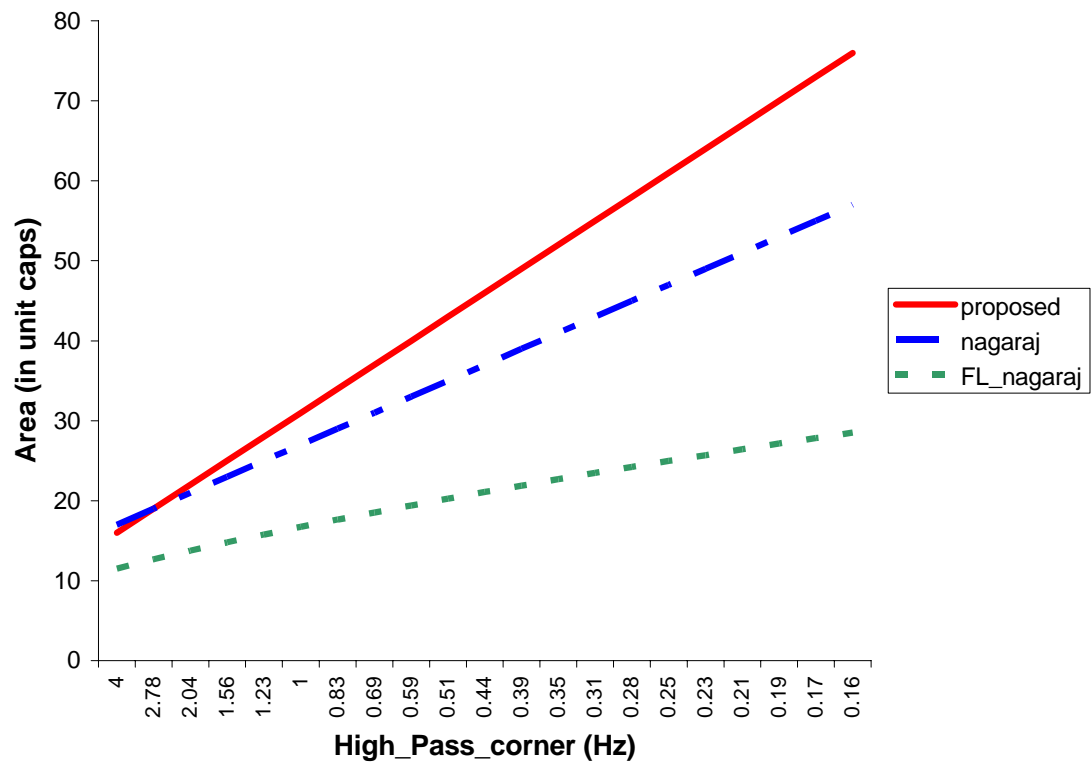


Fig. 4-19: Capacitor area comparisons

Fig. 4-19 compares the capacitor area of the three structures. The FL-Nagaraj structure is by far the best because we have three capacitor ratios to implement the large time constant.

Finally, Fig. 4-20 compares the noise of the three structures. The Nagaraj LPF has the worst performance because of the use of buffers, which contribute most of the noise. The FL-Nagaraj structure is competent with the proposed HPF.

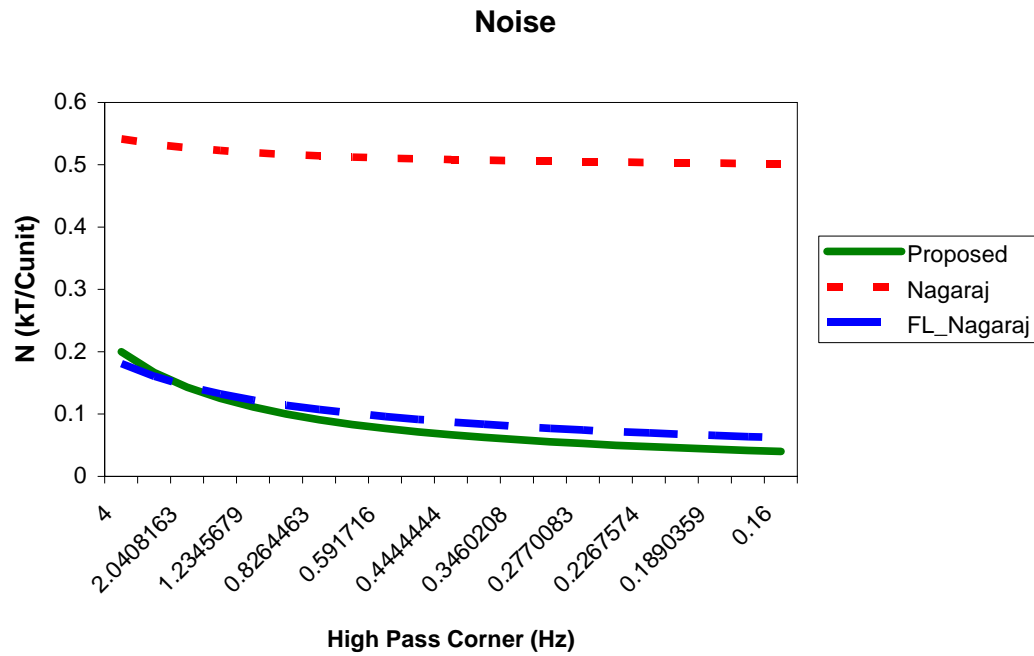


Fig. 4-20: Noise comparison plots



## **4.8 Conclusions**

In applications where a stand alone HPF is required, the topology proposed in this chapter definitely saves power. Up to cutoff frequency of 0.6Hz, the proposed structure consumes minimum power. Noise performance also exceeds the existing topologies. The main disadvantage comes up in capacitor area where three big capacitors are being used. Both the Nagaraj and the FL-Nagaraj structure use just one big capacitor. Thus the proposed topology trades of power and noise against area in comparison with existing topologies for implementing a stand-alone high pass SC filter.

## CHAPTER V

### PRE-AMP DESIGN

#### 5.1. Introduction and Specifications

Except in some niche applications, stand alone high pass filters and differentiators are simply not used. Usually, they are used in conjunction with other circuits. In this chapter, we shall design biomedical pre-amplifiers using the proposed high pass filter and compare it with the conventional structures. Given below are the pre-amp specifications.

1. Supply Voltage = 1.6V (+/- 0.8V)
2. Clock Frequency = 2.5 KHz
3. Gain = 10
4. High pass corner = 4Hz and 0.159
5. Max tolerable error for HP Corner = 3% for 4Hz, 5% for 0.159Hz
6. Low pass corner = 200Hz  $\pm$  3%
7. Output Swing = 1.6V<sub>p-p</sub>
8. Input signal range (amplitude) = 4mV < V<sub>IN</sub> < 40mV
9. SNR > 30dB for 4Hz and SNR > 26dB for 0.159 HP Corner
10. Static Current consumption < 200nA
11. Minimum unit capacitor = 0.25pF
12. Minimum Transistor current = 10nA

Given below in Fig. 5-1 is the block diagram of the pre-amplifier.

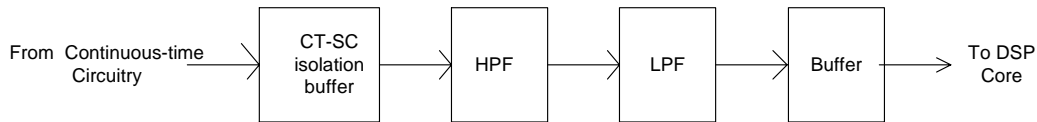


Fig. 5-1: Block diagram of pacemaker pre-amp

Either the LPF or the HPF will have a passband gain of 10. Either approach has its advantages. If the HPF is given a gain of 10, then we get better noise performance at the expense of power consumption. If the LPF is given a gain of 10, we get lower power consumption at the expense of noise. One reason is that the HPF sees larger load capacitors than the LPF and these load capacitors will be multiplied by the gain when loading on the OTA is considered. The other reason is that now the swing on the OTA in the HPF is reduced and this also has the potential to save power. As will be demonstrated in the following sections when we design the pre-amp, we will be able to meet the noise specifications even if the gain of 10 is given to the LPF. Thus to minimize power consumption, the LPF must have a passband gain of 10.

## 5.2 Pre-amp Using the Proposed HPF

Given in Fig. 5-2 is the schematic of the pre-amp using the proposed HPF.

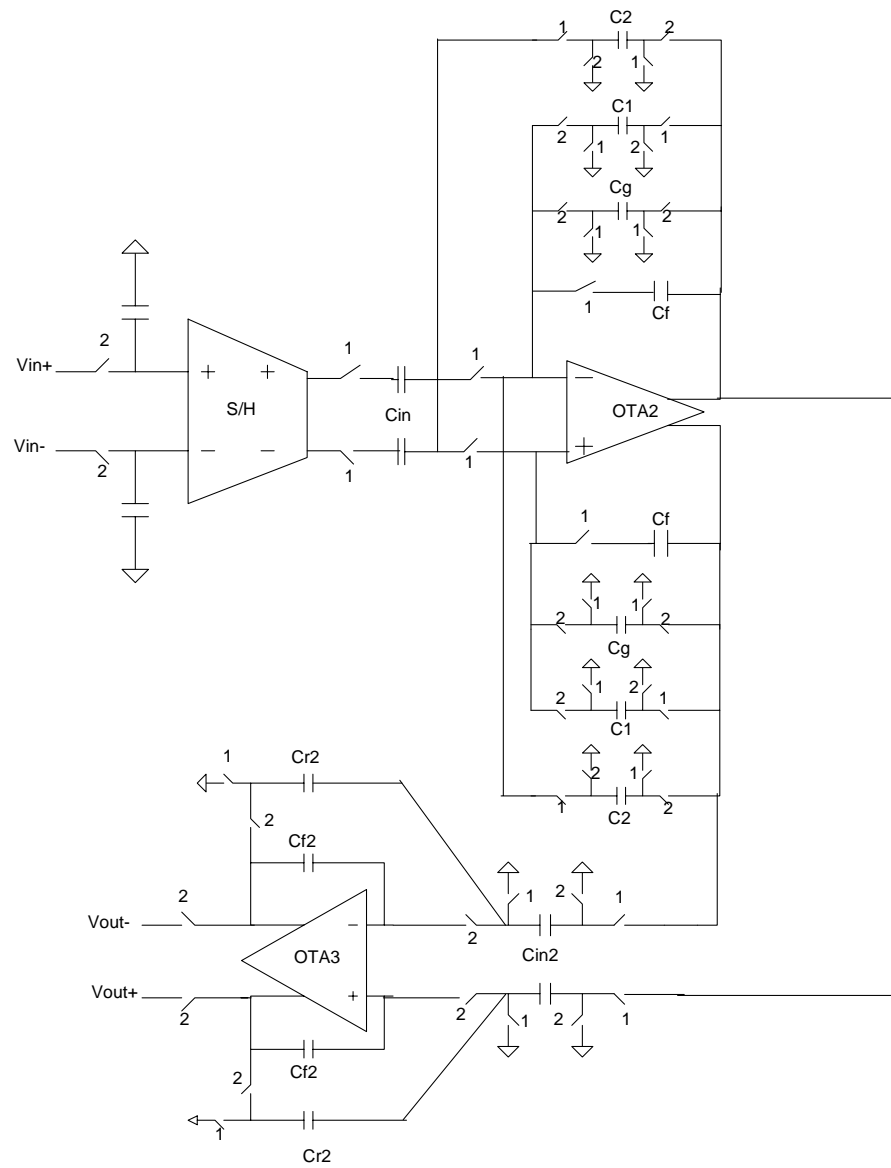


Fig. 5-2: Pre-amp using proposed fully differential HPF

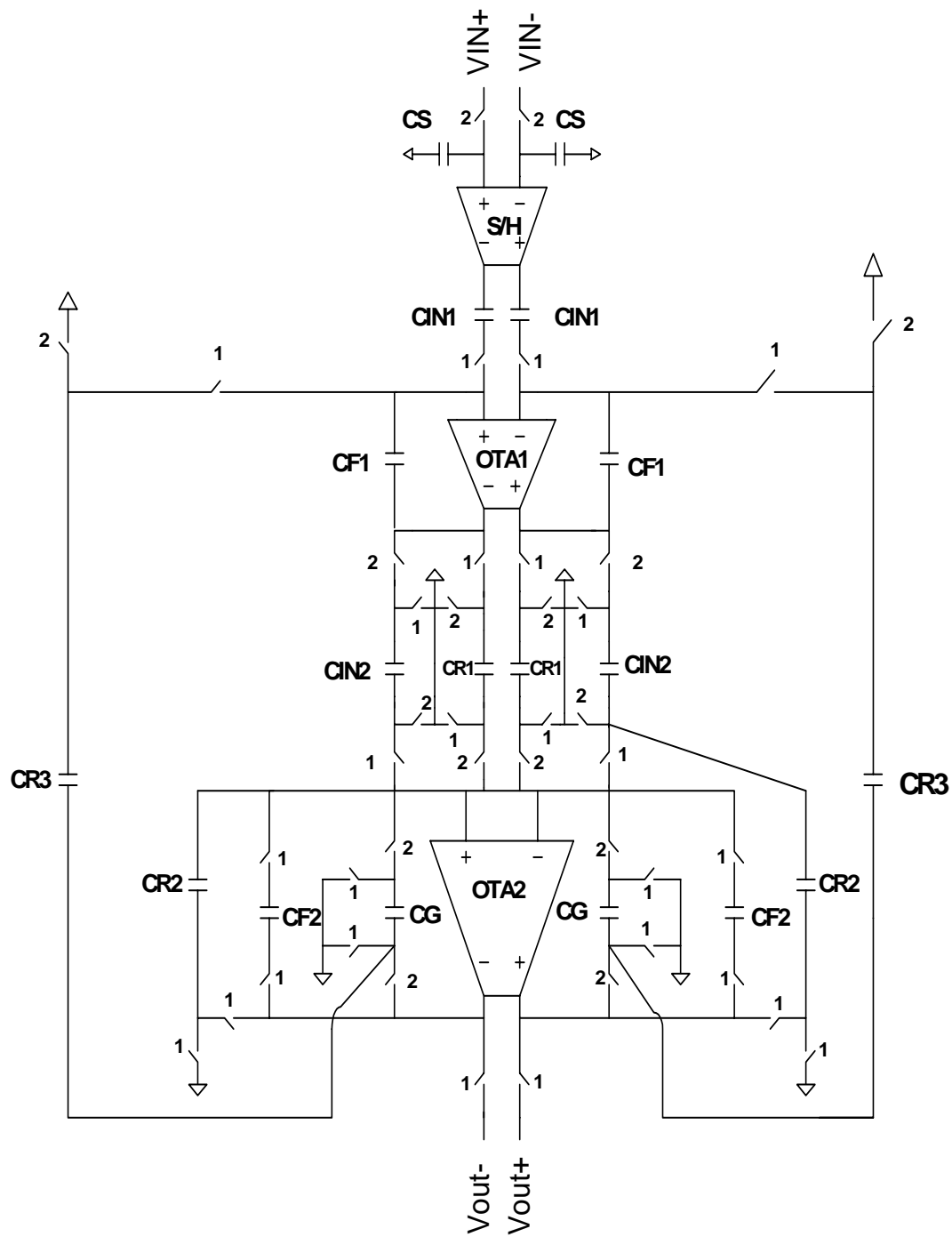


Fig. 5-3: Pre-amp using attenuated feedback HPF and OTA reuse

The first stage is a S/H, the second is a HPF and the third is an LPF with a gain of 10. As demonstrated in section 4.4.4 of Chapter IV, OTA 2 is heavily strained because of the heavy loading ( $C_{IN}$ ) well as a large swing between clock phases. As a result, a large GBW is demanded of it. The HPF structure being used in Fig. 5-2 is more suitable for stand-alone applications. For use in a pre-amp, we must use the HPF structure presented in Fig. 4-11, which uses two OTAs. Thus the pre-amp of Fig. 5-2 is slightly modified as shown in Fig. 5-3.

OTA 1 performs just the differentiation, while OTA 2 performs two functions. In phase 1, it performs low pass filtering and in phase 2, it performs attenuation for the high pass filter. Thus OTA 2, which is mainly for the low pass filtering is being re-used in its idle phase to perform the attenuation for the HPF.

The defining equations for a 4Hz HPF cutoff and a 200Hz LPF cutoff follow below. For a high pass corner, the equation is

$$\frac{C_{F1}C_G}{C_{R1}C_{R3}} = 100. \quad (5.1)$$

For a low pass cutoff, the equation is

$$\frac{C_{F2}}{C_{R2}} = 1.5. \quad (5.2)$$

And the gain is given by

$$\frac{C_{IN2}}{C_{R2}} = 10. \quad (5.3)$$

We use a unit capacitor of 0.25p. We choose the capacitors in such a way that the smallest possible capacitors are used to perform common centroid matching. Table 5-1 gives the capacitor values.

Table 5-1: Capacitor values for Fig. 5-3 for a 4 Hz high pass corner

C <sub>in</sub>	C <sub>f</sub>	C <sub>r</sub>	C <sub>r1</sub>	C <sub>r2</sub>	C <sub>g</sub>	C <sub>f2</sub>	C <sub>in2</sub>
2.5p	2.5p	0.5p	0.25p	0.25p	2.5p	.75p	5p

C<sub>in</sub>, C<sub>f</sub>, C<sub>r2</sub> are matched in one cluster, C<sub>r1</sub>, C<sub>g</sub> in another and C<sub>r</sub>, C<sub>f</sub> and C<sub>in2</sub> in the last.

The loading on OTA 1 during phase is given by

$$C_{TOT} = C_{IN1} + C_{R1} + C_{cmfb} + 0.2C_{F1} = 3.75 pF. \quad (5.4)$$

During phase 2 it is C<sub>IN2</sub>, which is 5pF. Further, it was assumed that the bottom plate parasitic capacitances (on C<sub>F1</sub>) equal roughly 20% of the capacitor value. Thus the maximum loading in this case is during phase 2 and equals 5pF.

The loading on OTA 2 during phase 1 assuming a load capacitance of 0.5pF for the next stage is

$$C_{TOT2} = 10 \times (C_{cmfb} + C_L) + C_{IN2} = 15 pF. \quad (5.5)$$

The loading during phase 2 is only C<sub>R3</sub>, which is a small capacitance. The maximum loading is during phase 1 and equals 15pF.

Assuming that 5 time constants are required for 1% settling error, the trans conductance of OTA 1 is given by equation (5.6).

$$g_{m1} = 5 \times 2f_{CLK} \times C_{IN2} = 0.125\mu A/V. \quad (5.6)$$

For OTA 2, the transconductance is given by

$$g_{m2} = 10f_{clk} \times C_{eff2} = .375\mu A/V. \quad (5.7)$$

From the equations in Chapter IV, OTA 1 and OTA 2 must have a gain in excess of 1000 (for 1% error in gain). Thus a simple current mirror OTA is not suitable. A folded-cascode is required. From the equations in Chapter II, a current of 5nA is required to flow in each transistor of the input differential pair for a trans conductance of 0.125uA/V and 15nA is required for a trans conductance of 0.375uA/V. 5nA is below the minimum specified current of 10nA and thus the concerned OTA 1 must carry 40nA (10nA through each branch). OTA 2 must carry a current of

$$I = 15 + 15 + 10 + 10 = 50\text{nA}.$$

The first stage S&H needs to carry 40 nA. Thus the total power consumption equals

$$I_{\text{total}} = 40+40+50 = 130\text{nA}.$$

Similarly for a 0.159 Hz cutoff frequency, it can be shown that the capacitor values are as shown in Table 5-2.

Table 5-2: Capacitor values for Fig. 5-3 for a 0.159 Hz high pass corner

Cin	Cf	Cr	Cr1	Cr2	Cg	Cf2	Cin2
12.5p	12.5p	0.5p	0.25p	0.25p	12.5p	.75p	5p



The other circuit parameters for the 0.159 Hz cutoff can be shown to be:

$$G_{m1} = 0.4 \text{ uA/V}$$

$$I_{D1} = 16.5 \cdot 2 + 10 \cdot 2 = 53.5 \text{ nA}$$

$$I_{D2} = 50 \text{ nA (requirements remain the same)}$$

$$\text{Total power} = 143.5 \text{ nA}.$$

For simulations, it will be noted that the actual power consumption will be slightly higher. These equations are for gaining insight and intuition into tradeoffs between time constants and power consumption.

### 5.2.2 Noise analysis

We will finally round off with the noise analysis. The expressions for noise power of a HPF stage, an LPF stage have already been derived in Chapter IV, section 4.6. It was proved that the noise from the switches is far greater than that from the OTAs, i.e. the  $kT/C$  expression dominated the noise. In the pre-amp here, we just combine those results to get the complete expression for noise. The total output referred noise of the pre-amp is

$$v_{n,in}^2 = \frac{kT}{C_S} + 2 \frac{kT}{C_{IN1}} + N_{HPF} + N_{LPF}. \quad (5.8)$$

For complete expressions of  $N_{HPF}$  and  $N_{LPF}$ , the reader is referred to section 4.6 in Chapter IV.  $kT/C_{in1}$  is the result of the white noise from the switch and the white noise from the S/H stage.  $C_S = 5 \text{ pF}$  is added to the input stage. Thus the complete noise power is given by

$$\begin{aligned}
N_{0.159Hz} &= 23.4 \times 10^{-10} V^2 \\
N_{4Hz} &= 49 \times 10^{-10} V^2.
\end{aligned}
\tag{5.9}$$

The values above are for the input referred noise. The smallest signal that is input to the pre-amp equals 4mV and the largest equals 40mV. For worst case SNR, we must use the smallest input signal. Thus the SNR values equal

$$\begin{aligned}
SNR_{0.159Hz} &= 38dB \\
SNR_{4Hz} &= 32dB.
\end{aligned}
\tag{5.10}$$

These values exceed the specifications.

### 5.3 Pre-amp Using the FL-Nagaraj Biquad

A single ended version of the biquad is given below in Fig. 5-4. The design equations to determine the power consumption and capacitor sizes will be the same for the differential ended and the single ended cases.

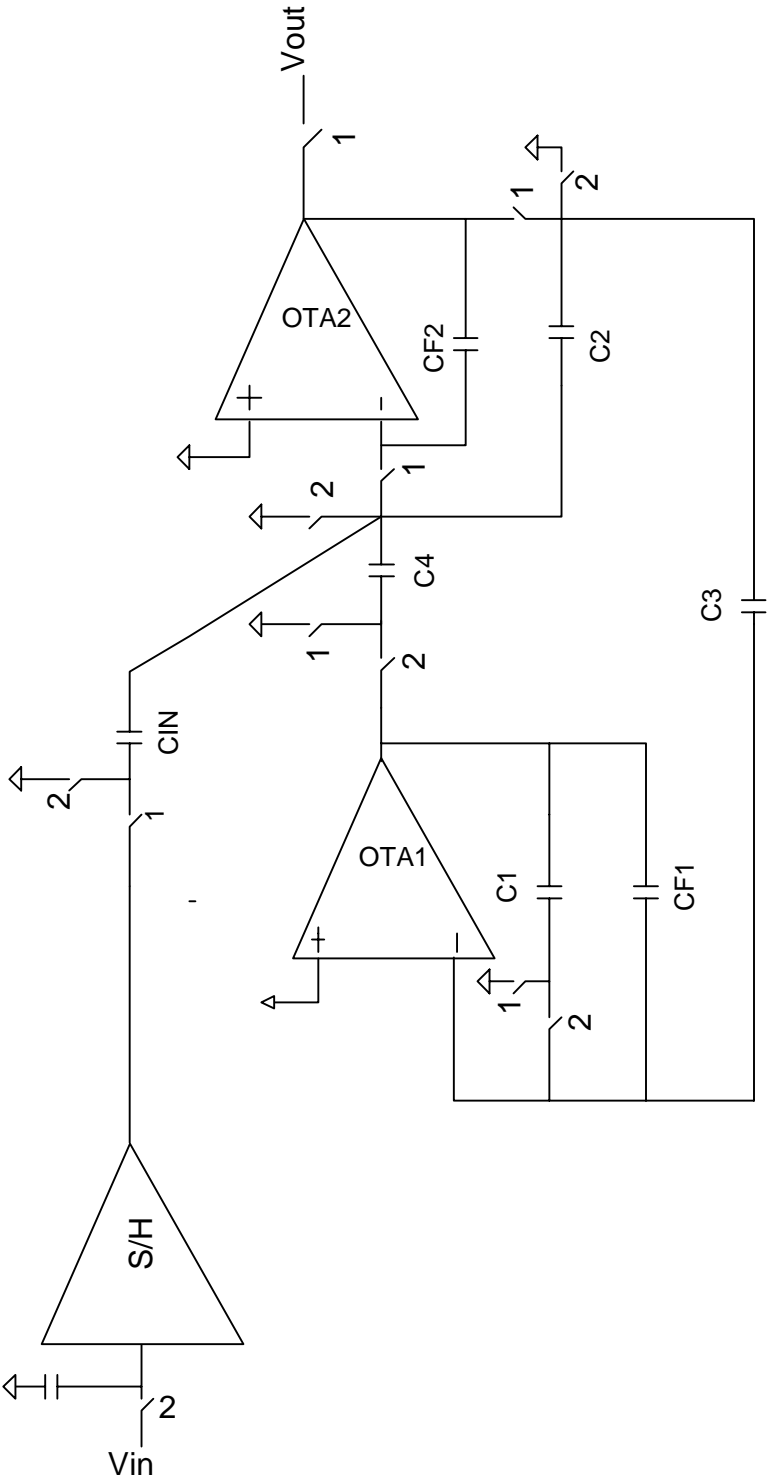


Fig. 5-4: Pre-amp using FL biquad and Nagaraj integrator

The following design equations apply for the design.

The gain is given by

$$G = \frac{C_{IN}}{C_2} = 10. \quad (5.11)$$

The high pass corner is given by

$$\rho_{HPF} = \frac{C_{F1}^2 C_2}{C_1 C_3 C_4} f_{clk}^2. \quad (5.12)$$

Since, OTA 2 must implement the gain stage, it is best to keep  $C_2$  as small as possible, because that would keep  $C_{IN}$  small and thus prevent loading OTA 2 too much.

The low pass corner is given by

$$\rho_{lpf} = \frac{C_2}{C_{F2}} f_{clk}. \quad (5.13)$$

Thus for a 4Hz high pass corner, we have

$$100 = \frac{C_{F1}^2 C_2}{C_1 C_3 C_4} = \frac{C_{F1}^2}{C_1 C_3} \quad (5.14)$$

$$\frac{C_2}{C_{F2}} = 1.5.$$

Thus the capacitor values for a 4Hz design (assuming common-centroid matching and 0.25p unit capacitors) are given in Table 5-3.

Table 5-3: Capacitor values for Fig. 5-4 for a 4 Hz high pass corner

$C_{IN}$	$C_1$	$C_2$	$C_3$	$C_4$	$C_{F1}$	$C_{F2}$
5p	0.5p	0.5p	0.5p	0.5p	5p	.75p

The clusters to be matched are  $C_1$ ,  $C_3$ ,  $C_{F1}$  and  $C_2$ ,  $C_4$ ,  $C_{F2}$ ,  $C_{IN}$ . The capacitor values above are the minimum that ensure common centroid. OTA 1 and OTA 2 both need high gain, as was discussed earlier in Chapter III, section 3.6.2. Both need to be folded- cascode, which can easily attain the required gain.

OTA 1 is minimally loaded during both phases. The total load of OTA 1 is

$$C_{eff1} = C_3 + C_4 + C_{cmfb} = 1.5 pF. \quad (5.15)$$

Thus OTA 1 can carry the minimum current of 40nA.

OTA 2 is loaded effectively by

$$C_{eff2} = C_{IN} + 10 \times (C_{cmfb} + C_3 + C_L) = 20 pF. \quad (5.16)$$

$C_1$  is the loading of the next stage and is assumed at 0.5p. The  $g_m$  required thus can be calculated as

$$g_{m2} = 2 \times 5 \times f_{clk} \times C_{eff2} = 0.5 \mu A / V. \quad (5.17)$$

Thus OTA 2 requires a total current of 60nA ( $20 \times 2 + 10 \times 2$ ) to attain the required  $g_m$ .

The total current is 140nA. If the high pass corner required reduces to 0.159 Hz, the power consumption does not change as the loading is not affected by  $C_{F1}$ , which effectively sets the time constant. Thus the power consumption always remains at 140nA. The Capacitors required for a 0.159 Hz cutoff are given in Table 5-4.

Table 5-4: Capacitor values for Fig. 5-4 for a 0.159 Hz high pass corner

$C_{IN}$	$C_1$	$C_2$	$C_3$	$C_4$	$C_{F1}$	$C_{F2}$
5p	0.5p	0.5p	0.5p	0.5p	24.5	075p

### 5.3.2 Noise Analysis

The expression for input referred noise is given by

$$v_{n,in}^2 = \frac{kT}{C_S} + 2 \frac{KT}{C_{IN}} + N_{BIQUAD}. \quad (5.18)$$

$N_{BIQUAD}$  has already been derived in section 4.5.3 of Chapter IV. We just have to punch in the values.

$$\begin{aligned}
 v_{n,in,0.159Hz}^2 &= 41.4 \times 10^{-10} V^2 \\
 SNR_{0.159Hz} &= 33dB \\
 v_{n,in}^2 &= 77 \times 10^{-10} V^2 \\
 SNR_{4Hz} &= 30dB.
 \end{aligned} \quad (5.19)$$

These results exceed the specifications.

## 5.4 The Nagaraj Low Pass Filter

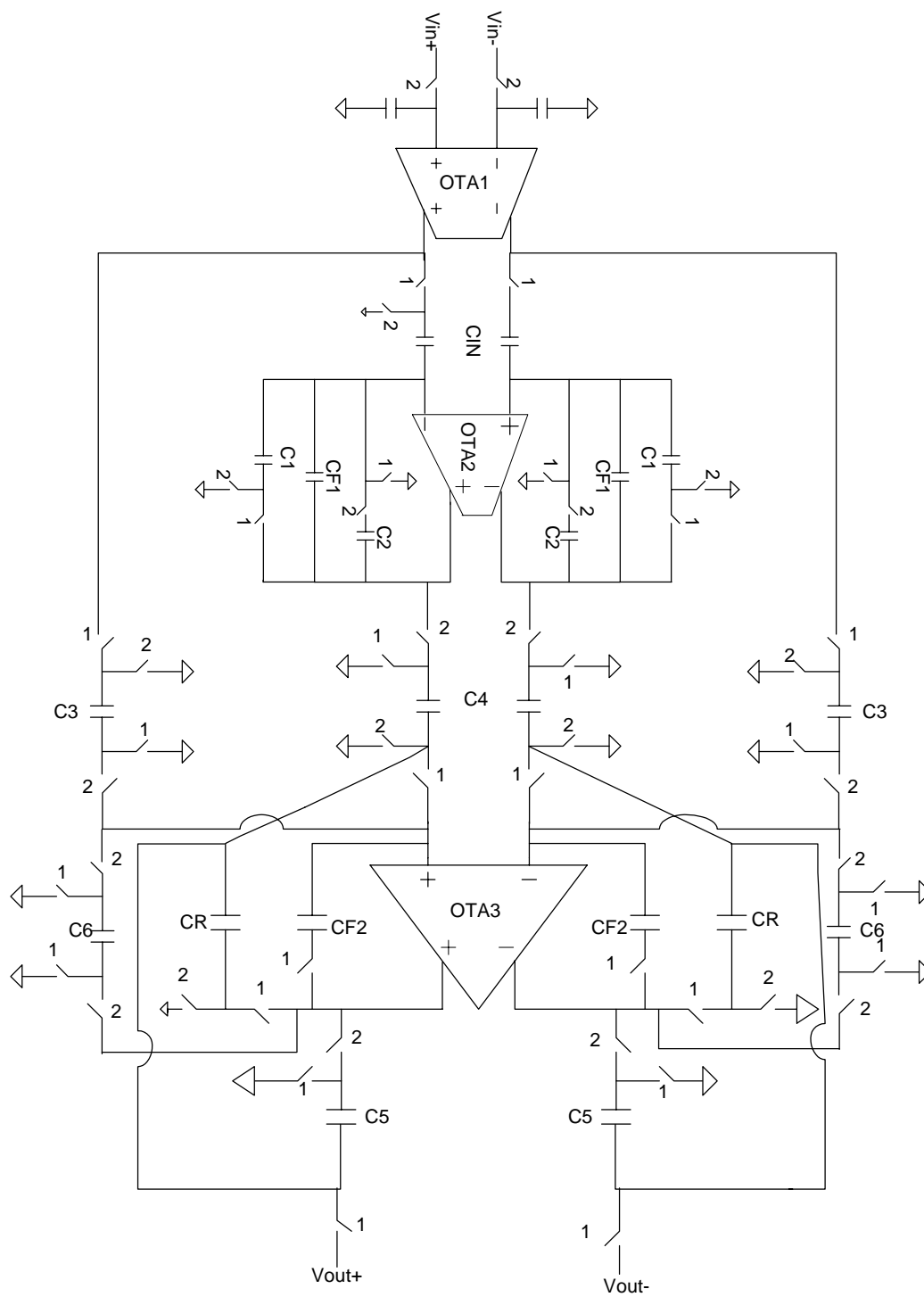


Fig. 5-5: Pre-amp implementation using Nagaraj LPF and OTA reuse

Fig. 5-5 shows the pre-amp using the Nagaraj low pass filter. OTA 1 performs the buffering, OTA 2 is the Nagaraj low pass filter. OTA 3 performs buffering (1-LPF=HPF) for the high pass function in phase 2. It performs the low pass filtering with gain in phase 1. The design equations follow below.

The high pass corner is given by

$$\rho_{HPF} = f_{clk} \frac{C_1 C_2}{C_{F1}^2} \frac{1}{\left(1 + \frac{C_1}{C_{F1}}\right) \left(1 + \frac{C_2}{C_{F1}}\right)}. \quad (5.20)$$

The gain of the high pass filter is given by

$$G_1 = 1 = \frac{C_{IN}}{C_1} = \frac{C_3}{C_6}. \quad (5.21)$$

The gain of the low pass filter is given by

$$G_2 = 10 = \frac{C_4}{C_R} = \frac{C_5}{C_R}. \quad (5.22)$$

The low pass corner is determined the ratio between

$$1.5 = \frac{C_{F2}}{C_R}. \quad (5.23)$$

For a high pass corner of 4 Hz, the values of the capacitors are given in Table 5-5.



Table 5-5: Capacitor values for Fig. 5-5 for a 4 Hz high pass corner

$C_{IN}$	$C_{F1}$	$C_{F2}$	$C_R$	$C_1$	$C_2$	$C_3$	$C_4$	$C_5$	$C_6$
0.5p	4.5p	0.75p	0.5p	0.5p	0.5p	0.5p	5p	5p	0.5p

The clusters to be matched are  $(C_{in}, C_{F1}, C_1, C_2)$ ,  $(C_4, C_5, C_R, C_F)$  and  $(C_3, C_6)$

Thus assuming a unit capacitance of 0.25p, the above values ensure that the smallest possible capacitors are used for common centroid matching.

The DC gain specifications of both OTA 2 and OTA 3 necessitate the use of folded-cascode amplifiers just as was discussed in Chapter III.

Now let's consider the loading. OTA 2 is mainly loaded during phase 2. The loading during phase 2 is

$$C_{eff2} = C_4 + C_{IN} + C_{cmfb} = 6pF. \quad (5.24)$$

This corresponds to a  $g_m$  that is well below the minimum. So OTA 2 can carry 40nA of current. OTA 3 is loaded mainly during phase 1. The loading is given by

$$C_{eff3} = C_4 + C_5 + 10(C_{CMFB} + C_{load,nextstage}) = 20pF. \quad (5.25)$$

This corresponds to a  $g_m$  of 0.5uA/V. Thus the power consumption of OTA 2 is  $(20 + 20 + 10 + 10 = 60nA)$ . Thus the total power consumption of this pre-amp is 140nA. The power consumption does not change with decreasing high pass corner, because decreasing high pass corner, only increases the value of  $C_{F1}$  which does not load any OTA.

For a 0.159 Hz cutoff, the capacitor values are given in Table 5-6.

Table 5-6: Capacitor values for Fig. 5-5 for a 0.159 Hz high pass corner

$C_{IN}$	$C_{F1}$	$C_{F2}$	$C_R$	$C_1$	$C_2$	$C_3$	$C_4$	$C_5$	$C_6$
0.5p	24.5p	0.75p	0.5p	0.5p	0.5p	0.5p	5p	5p	0.5p

Finally, from noise computations, we can compute the SNR for a minimum input signal of 4mV to equal 26dB.

As discussed in section 4.5.2 of Chapter IV, the SNR does not seem to change with time constant. We will now discuss some non-ideal effects in SC circuits that might cause errors in large time constants.

## 5.5 Charge Injection and Leakage

Charge injection is a complex problem and not a well-modeled phenomenon. In Cadence, charge injection is modeled by assuming that half the channel charge flows out of the source and the other half out of the drain of a switch whenever it goes off. Thus in a fully differential circuit, charge injection appears as a common mode offset and its effect is seen to be negligible in simulations. Even in single ended circuits, charge injection can be easily cancelled in simulations by using dummy transistors. In reality however, the utility of dummy transistors is debatable. Dummy transistors work in simulations because of the assumption that half the channel charge flows out the source

and the other half out the drain. In reality, what percentage of the charge flows out the drain or source depends on many factors including the node voltages including the impedances seen looking out the switch terminals. The best way to reduce charge injection is to use minimum dimensions in the devices, which however might increase the leakage.

Leakage did not seem to be much of an issue in simulations. There are two kinds of leakage that we can expect:

1. The finite OFF resistance of the switches can cause them to conduct small currents which when integrated over a large enough time(as in large time constants) can cause non-negligible errors. However, the OFF resistance of the switches (MOS transistor in accumulation) was measured in simulations (single transistor) to be high enough so that this was not a noticeable or measurable problem.
2. Reverse biased p-n junction currents: In a MOS transistors the reverse biased p-n junctions are the source-bulk and the drain-bulk currents. Simulation results indicated that these currents were quite negligible as to cause them to be un-measurable.

## **5.6 Clock Feed-Through**

It turns out that clock feed-through is the single most important non-ideal effect encountered in the design of large time constants. Clock feed-through occurs due to the non-idealities of the switch. Whenever, the switch makes a transition, charge is transferred via  $C_{GS/GD}$  of the switch transistor. When this charge flows through the integrating capacitor, it causes a change in the output. This charge is independent of the

signal level. It is only dependent on the clock swing and the values of the parasitic capacitors. Thus it does not cause any non-linearity. Rather, it causes an offset at the output. In single ended circuits, this offset could get to be a problem. In differential ended circuits, most of the clock feed through appears as a common mode voltage at the output and is compensated by the CMFB circuit. In differential ended circuits, clock feed through is greatly reduced as a common mode offset. Differential mode clock feed through occurs because of mismatches between the switches used in the two differential signal paths. If the signal paths are completely symmetric, clock feed through will manifest as a common mode output voltage and will be completely cancelled by the CMFB circuit. However, small mismatches always ensure that the two differential paths are never completely symmetric. It is this asymmetry that causes a differential mode clock feed-through. Usually the circuits are largely symmetric and thus differential mode circuits can operate at much lower frequencies than singled ended circuit. However, at even lower frequencies, even differential mode clock feed through becomes significant.

To analyze charge injection in a SC circuit, we must first identify the critical switches. The critical switches are usually to be found at the non-inverting input of the OTA, this being the most sensitive node in the circuit. The second thing we must understand is that, like charge injection, it occurs when the switches go off. Thus for NMOS switches, clock feed-through occurs during the falling edge of the clock. When the clock falls, charge flows through the  $C_{GS}$  or  $C_{GD}$  of the NMOS switch and then flows through the integrating capacitor, thus causing a voltage change at the output.

We will analyze a few circuits below for clock feed through to make our point more forcefully.

### 5.6.1 The Nagaraj structures

Consider the Nagaraj LPF in Fig. 5-6a.

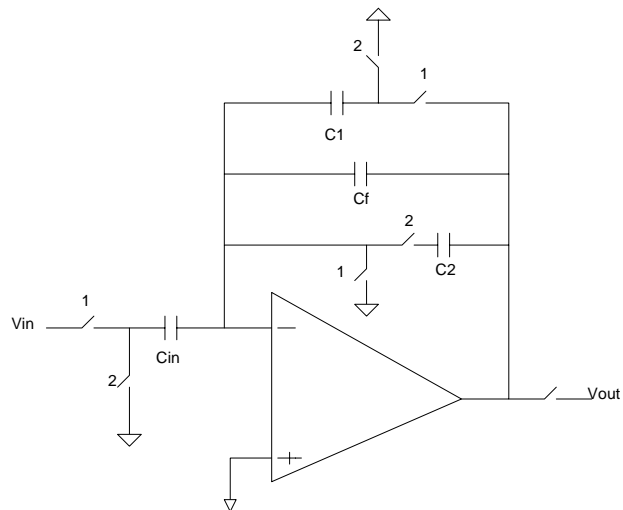


Fig. 5-6a: The Nagaraj LPF

The switches that are most responsible for clock feed-through are the two switches adjacent to  $C_2$ . In each case, whenever the switches go off, a small charge flows through  $C_F$  thus causing a small voltage error. In the appendix, a proof will be offered as to why the switches adjacent to  $C_1$  and  $C_{IN}$  do not cause quite as much error.

Now consider the Nagaraj integrator in Fig. 5-6b.

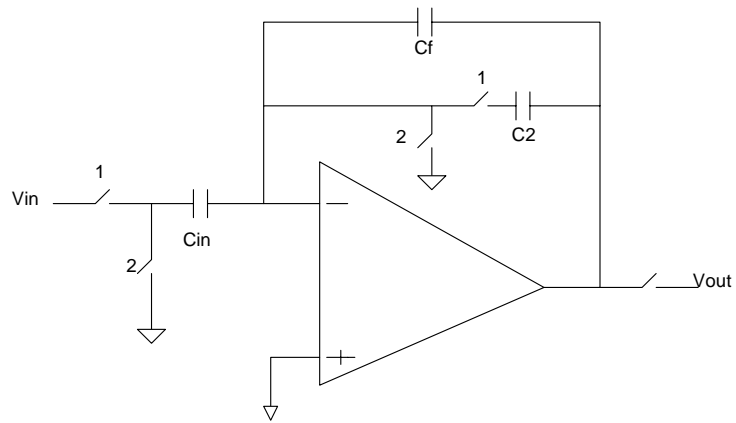


Fig. 5-6b: Nagaraj integrator

This structure has two sensitive switches. Both switches adjacent to  $C_2$  cause clock feed-through. Thus, it is the same as the Nagaraj LPF.

Now finally consider the proposed HPF structure, which we have used in our pre-amp. Use Fig. 5-6c as a reference.

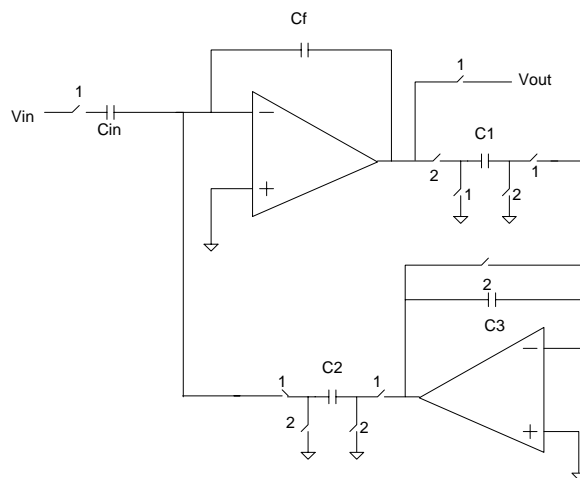


Fig. 5-6c: Proposed HPF

Here, the critical switch is the one operating in phase 1, adjacent to  $C_2$  to its left hand plate. When that switch goes off, a small charge flows through  $C_F$  causing a small error at the output.

## 5.7 Comparisons

The graphs in Figs. 5-7 and 5-8 compare the area and power consumption of the three structures discussed in this chapter.

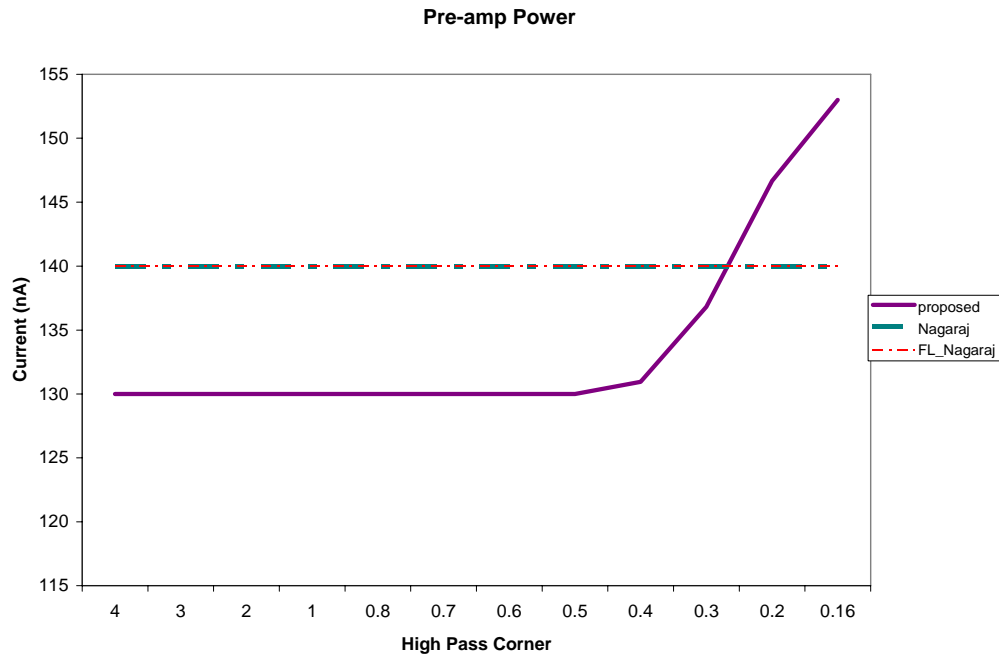


Fig. 5-7: Power consumption of the three pre-amps.  $I_{\text{NAGARAJ}} = I_{\text{FL-NAGARAJ}}$

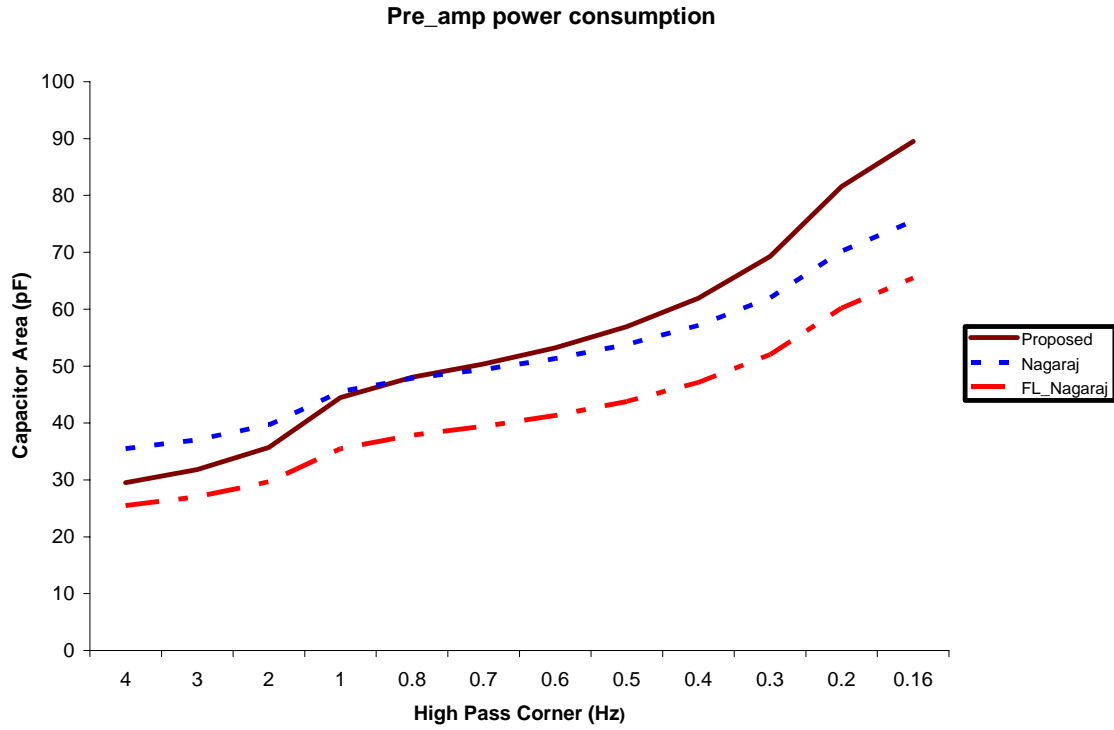


Fig. 5-8: Capacitor area of the three pre-amps

The power consumption of the Nagaraj LPF and the FL-Nagaraj biquad is the same and therefore, the plots are superimposed. As can be seen, for medium to large time-constants, the proposed HPF saves power, but for very large time-constants, conventional techniques consume lower power. The FL-Nagaraj biquad occupies the lowest area of all structures.



## 5.8 Layout

Fig. 5-9 shows the layout of the proposed HPF based pre-amp.

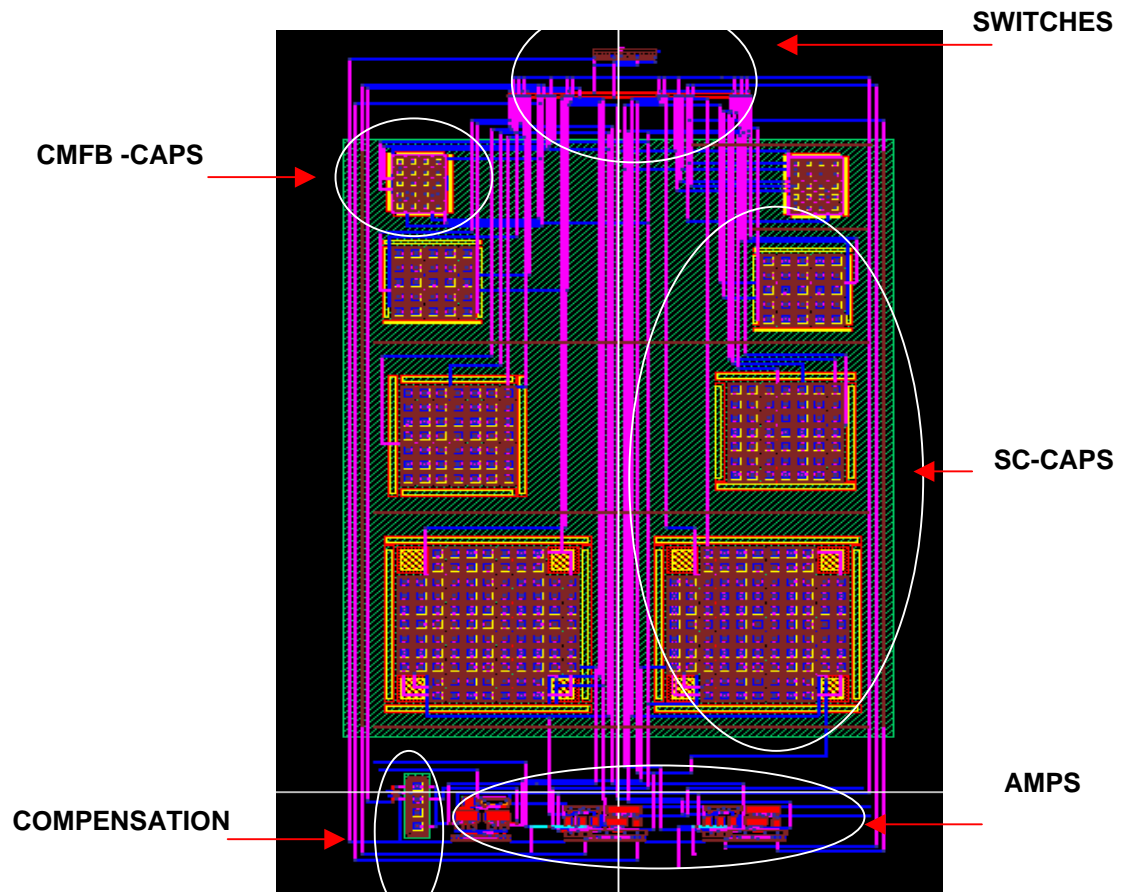


Fig. 5-9: HPF based pre-amp layout

## 5.9 Simulation Results

In this section, we present the simulation results for the three structures we have designed. We start with the proposed technique in section 5.9.1, the FL-Nagaraj biquad in section 5.9.2 and the Nagaraj LPF in section 5.9.3.

### 5.9.1. Proposed technique

The entire structure using the proposed technique was simulated. This schematic of this structure is shown in Fig. 5-3. A periodic steady state (PSS) analysis was performed for the circuit and the transfer function obtained. The results below show three plots, each of them focusing on one aspect of the transfer function, i.e. the low pass corner, the high pass corner and the passband gain.

Fig. 5-10a shows the plot of the transfer function focusing on the high pass corner at 0.159Hz. The plot shows that the corner is actually at 0.16Hz, which is very close to the 0.159 Hz that it was designed for.

Fig. 5-10b shows focuses on the low pass corner, which was designed to be at 200Hz. The actual corner is at 197 Hz. The slight error can be attributed to the approximation in converting from the z-domain to the s-domain.

Finally, Fig. 5-10c shows the entire frequency response of the proposed pre-amp.

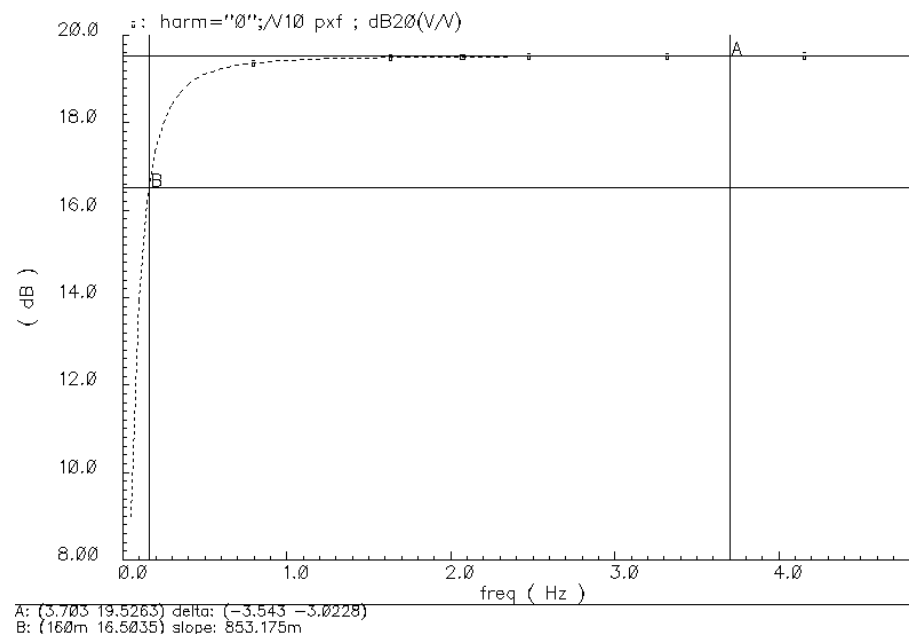


Fig. 5-10a: PSS response showing high pass corner

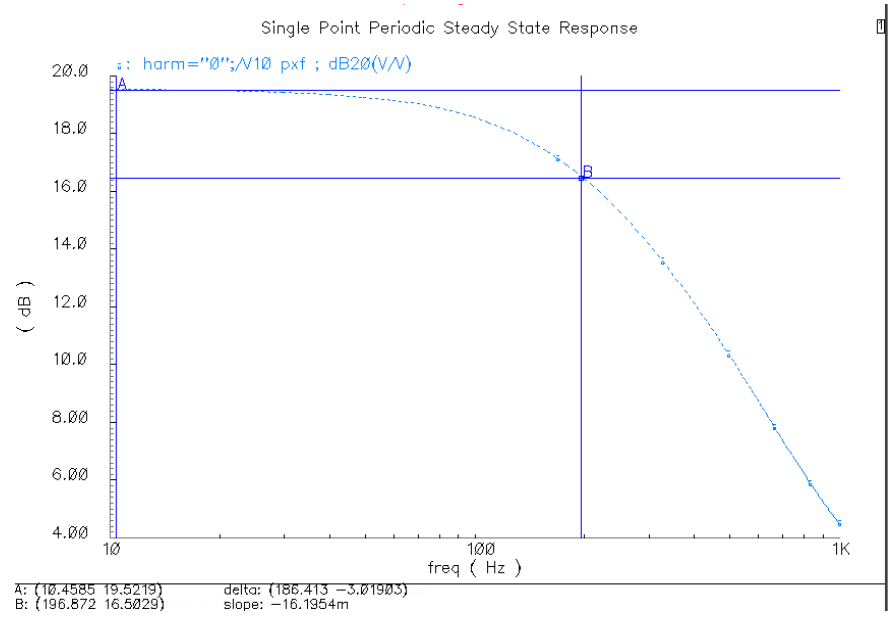


Fig. 5.10b: PSS response showing low pass corner

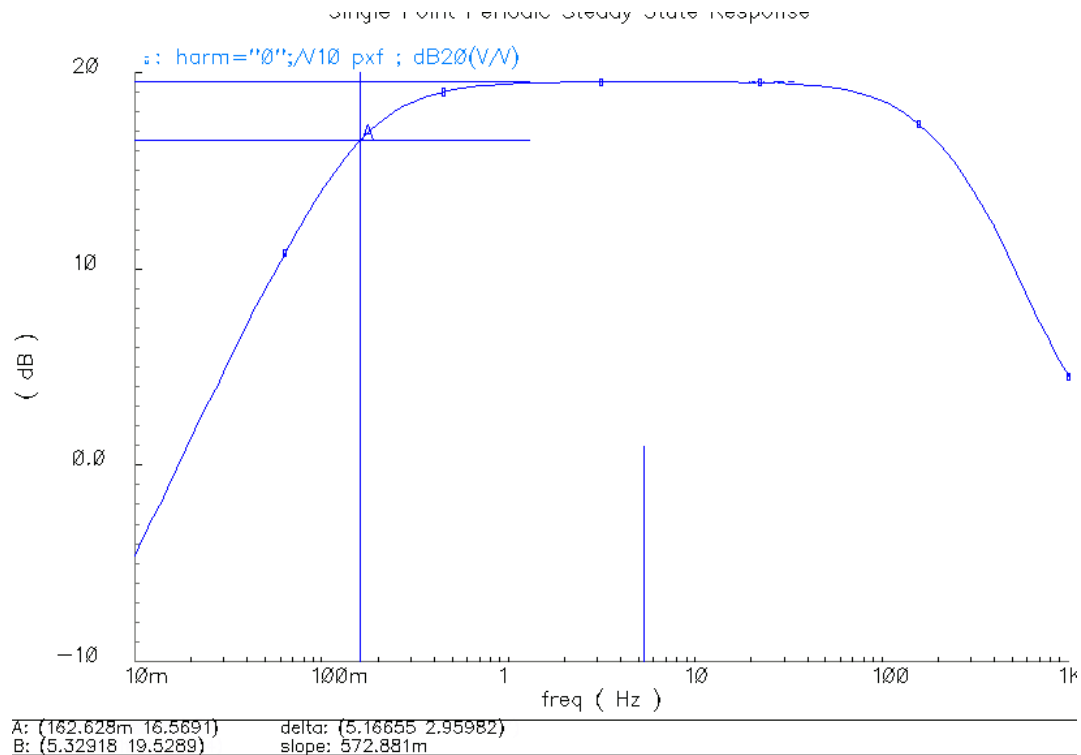


Fig. 5-10c: Complete PSS response for the proposed pre-amp

### 5.9.2 FL biquad using Nagaraj integrator

Fig. 5-11a and Fig. 5-11b show the transfer function for the FL biquad using the Nagaraj integrator. The reader is referred to Fig. 5-4 for the schematic. Fig. 5-11a indicates that the high pass corner is at 0.154 Hz, which is an error of 3% from the nominal 0.159Hz. Part of the error is because of the low frequency zero we had discussed earlier in section 3.2.2 of Chapter III. Fig. 5-11b shows the complete response with the markers indicating the low pass corner. The low pass corner is at 201.5 Hz, which is an error less than 1%.

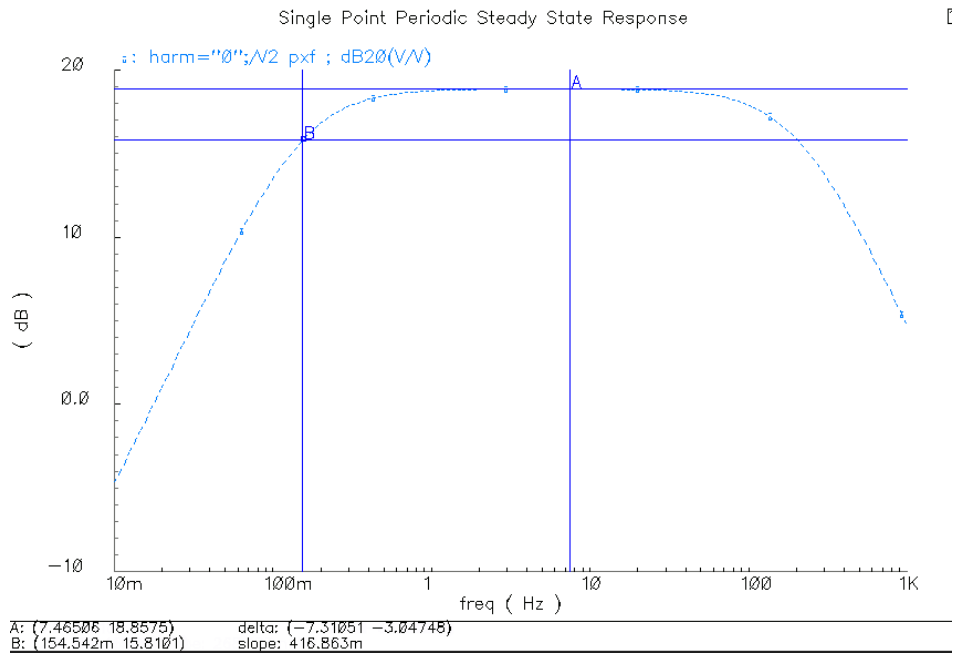


Fig. 5-11a: Complete PSS response for FL biquad showing the high pass corner

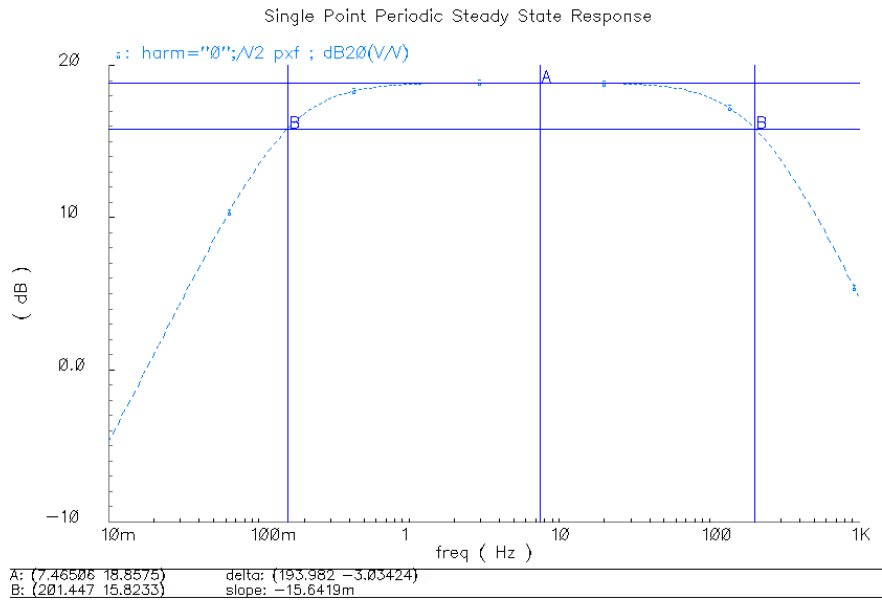


Fig. 5-11b: Complete PSS response of FL biquad showing the low pass corner

### 5.9.3 Nagaraj LPF

Fig. 5-12a and Fig. 5-12b show the transfer function for the pre-amp using the Nagaraj integrator. The reader is referred to Fig. 5-5 for the schematic. The high pass corner is at 0.164 Hz, which is an error of about 3% from the nominal 0.159 Hz. Fig. 5-11b shows the complete response with the markers indicating the low pass corner. The low pass corner is at 203 Hz, which is an error of 1.5% from the nominal 200 Hz.

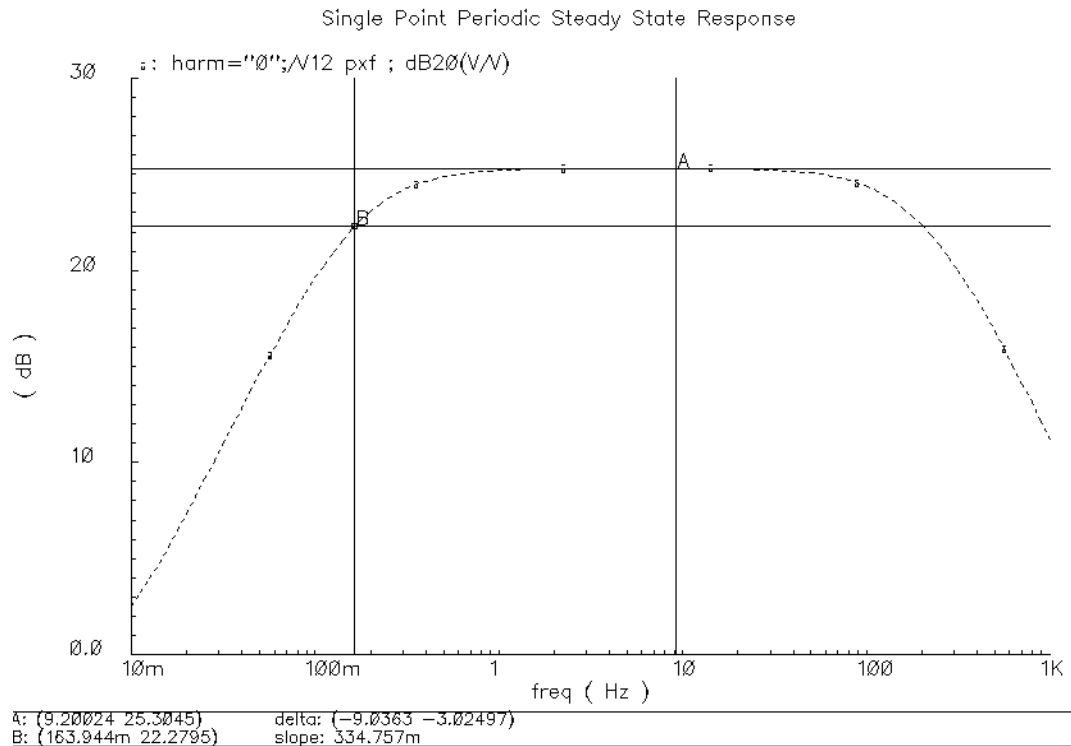


Fig. 5-12a: PSS response showing high pass corner

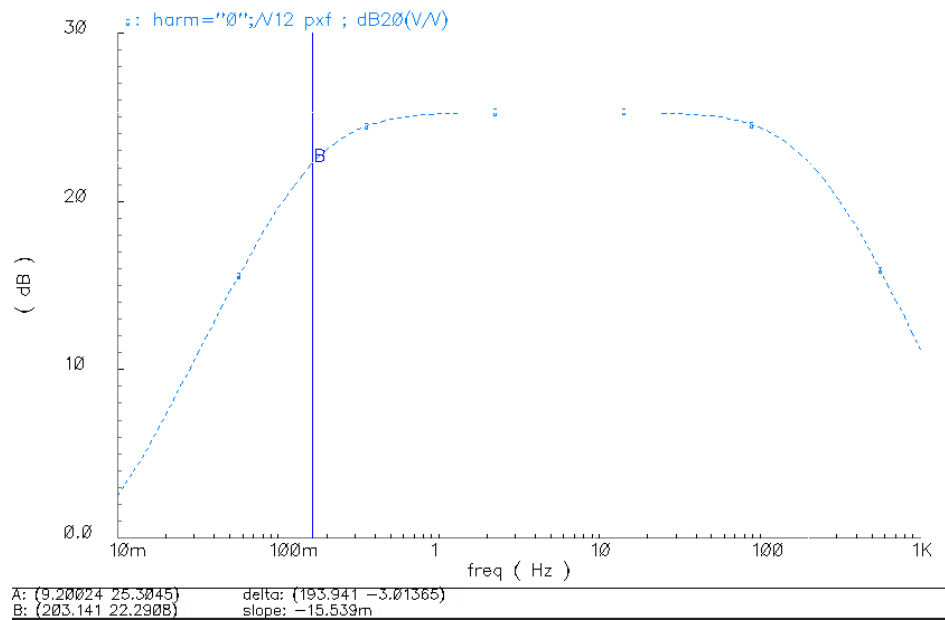


Fig. 5-12b: PSS response showing low pass corner

#### 5.9.4 More results from proposed pre-amp

The next few results are from the proposed pre-amp of Fig. 5-3. The graphs in Fig. 5-13a through 5-13d show the CMRR and PSRR of the proposed pre-amp in the presence of path and ratio mismatch. The pre-amp we have is fully differential (FD). In fully differential (FD) circuits, we are not interested in the output common mode voltage, which has no information and is always close to zero due to the action of the CMFB circuit. What we are interested in is the output differential voltage versus the input common mode voltage. Ideally, this value should be infinite. But in real FD circuits, there is always a mismatch between the two half circuits (the positive half and the negative half). It is precisely this mismatch that causes a finite CMRR. And for a fully differential circuit, the CMRR is defined by

$$CMRR = \frac{V_{OUT,DM}}{V_{IN,CM}}. \quad (5.26)$$

Mismatches in the transistor sizes in the OTA are removed by chopper stabilization to a large extent. However, chopper stabilization cannot remove the mismatches in the capacitors of the positive half circuit and the negative half circuit. Thus two kinds of mismatches have been introduced.

1. The capacitor ratios of both half circuits are the same. However, a mismatch in their absolute values is introduced. For instance suppose the capacitor ratio is 10 where the smaller capacitor is 0.5p and the bigger one is 5p. We deliberately introduce an error whereby the negative half circuit has capacitor values of 5.4p and 0.45p, while the positive half circuit has capacitor values of 0.55p and 5.5p. the ratios are the same, but the absolute capacitor values are different. This is called a path mismatch. This could go as high as 5%. The result is given in Fig. 5-12a. For simulation purposed, an error is introduced for every capacitor ratio.
2. A small mismatch is introduced in the capacitor ratios of the two half circuits. For instance, the capacitor ratio for the negative half circuit could be 9.9 while that for the positive half circuit could be 10. This kind of mismatch is usually limited to less than 1%. The result is given in Fig. 5-12b. Here too, an error is introduced in every capacitor ratio.



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Single Point Periodic Steady State Response [

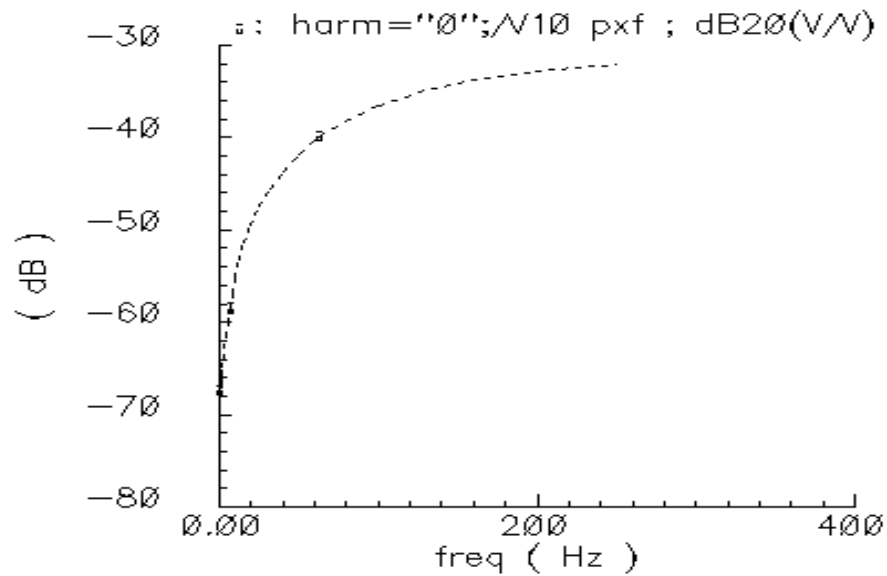


Fig. 5-13a: CMRR in presence of 5% path loading mismatch

Single Point Periodic Steady State Response [

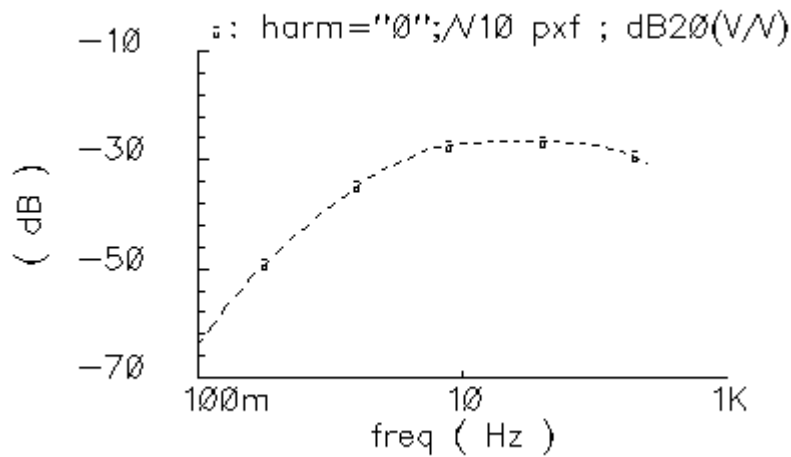


Fig. 5-13b: CMRR in presence of 1% ratio mismatch

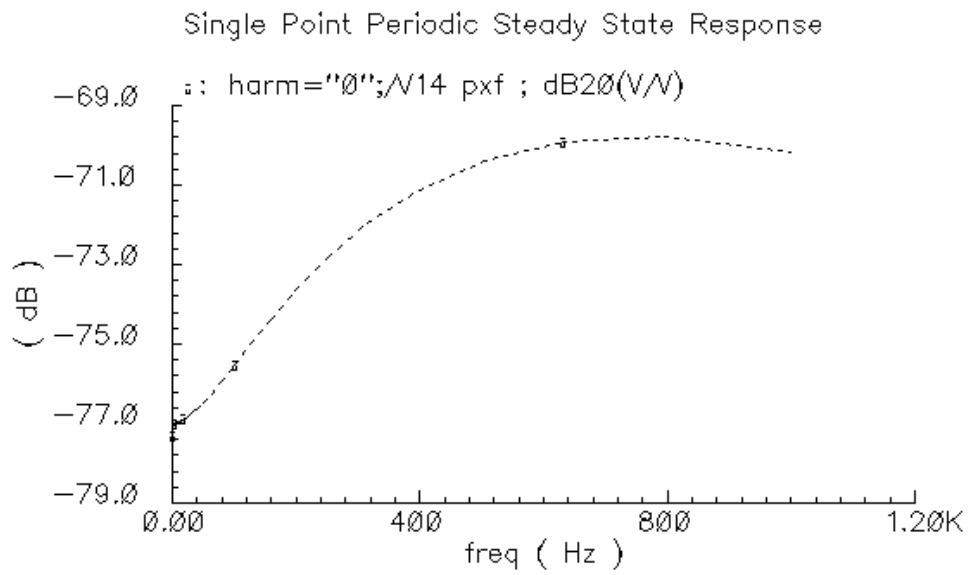


Fig. 5-13c: PSRR in presence of 5% ratio mismatch

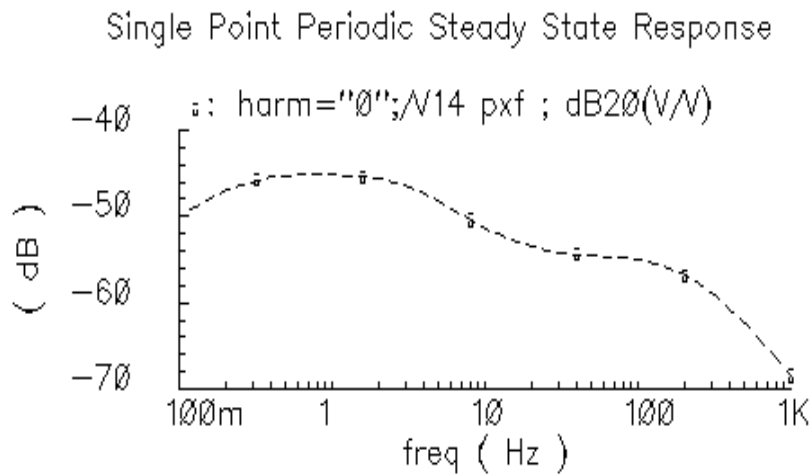


Fig. 5-13d: PSRR in presence of 1% ratio mismatch

### 5.9.5 Swing and linearity

The results below show transient simulations. The purpose is to measure the linearity. Switched-capacitor circuits have very high linearity. Most of the non-linearity comes from the finite DC gain and the parasitic junction capacitors, which are typically voltage dependent. Fig. 5-14a shows the output to a 40mV amplitude input sine wave at 100Hz, which is right in the middle of the bandwidth. The simulation indicates the output swing. Fig. 5-14b shows the DFT performed on the signal of Fig. 5-14a. Linearity is not much of an issue in SC circuits and in this case the linearity is much better than the noise.

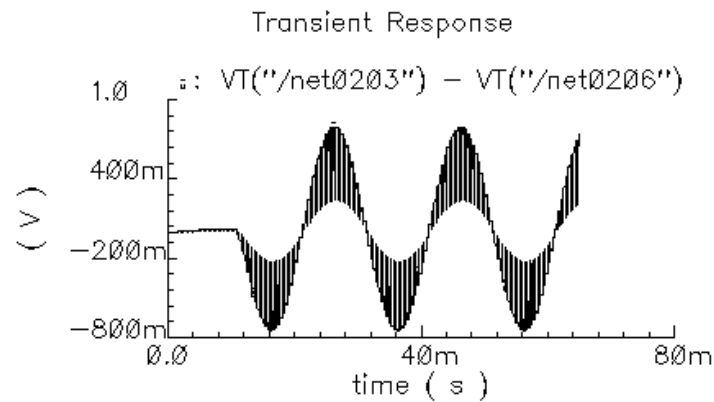


Fig. 5-14a: Demonstrating output swing in the OTA

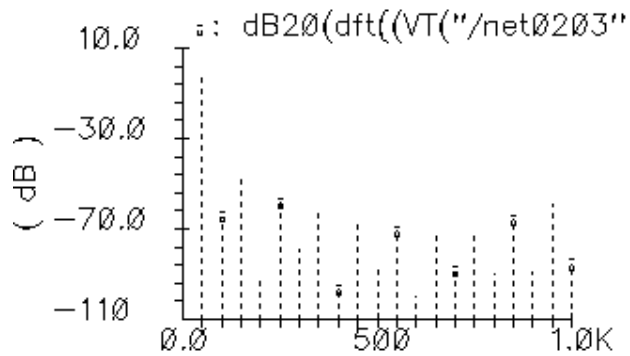


Fig. 5-14b: Demonstrating linearity via FFT. THD > 40dB

#### 5.9.6. Results from lab animal

Finally, real data obtained from a lab animal was given as an input to the pre-amp. The data was obtained courtesy of Lee Hudson of Biotronik. The results are shown in Fig. 5-15.

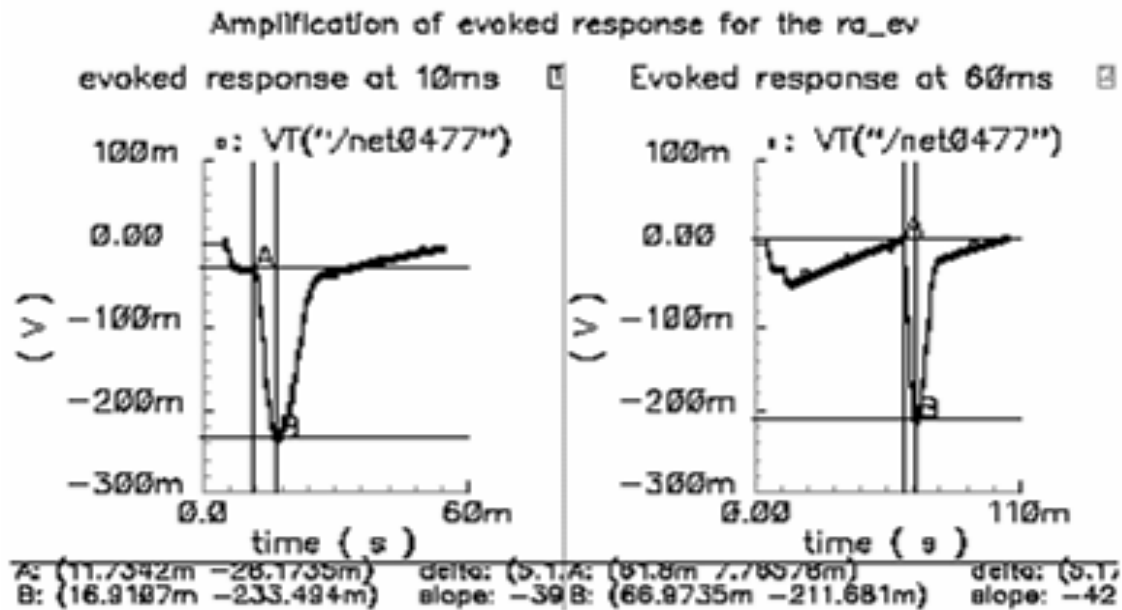


Fig. 5-15: Output to the evoked response

The signal on the left shows the output when the evoked response occurs almost after the pacing pulse is applied. The signal on the right is the output when the evoked response occurs much after the pacing pulse is applied. In pacemaker circuits, the power is turned off after processing and turned on just before the pacing pulse is applied. The SC circuit must use this short amount of time to quickly come to steady state before the evoked response is output by the heart. The simulation above tests how quickly and completely the SC circuit settles to steady state. Since the two profiles above are identical, it shows that the SC circuit settles to its steady state after power ON fairly quickly.

## CHAPTER VI

### CONCLUSIONS

This thesis sets out to design a pre-amp with the given specifications using a novel SC high pass filter, which can achieve large time constants. This topology is compared with two other pre-amp designs using conventional architectures. The result is that capacitor area is traded off for improvements in SNR and power consumption. The final designed pre-amp had the following characteristics:

- Technology AMI0.6u
- Supply 1.6V
- Voltage swing 800mVp-p
- Passband Gain 10
- HP Corner 0.159 Hz - 4Hz
- LP Corner 200 Hz
- Clock 2.5KHz
- Current 130nA – 150nA
- Cap Spread 50
- Error in time constant < 3%
- $SNR_{MIN} > 38 \text{ dB}$  (0.159Hz) and 32dB (4 Hz)

The following are the conclusions of this work:

- New HPF Structure suitable for small corner frequencies proposed.

- Structure consumes lower power for frequencies around 4Hz with small area penalty.
- HPF can be used with advantage for stand-alone applications.
- Differentiator based on HPF can be used on slow varying biomedical signals.
- HPF used in pre-amp trades off area for better noise and lower power for some applications.

For very low frequencies, the FL biquad is superior in almost all aspects.

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## VITA

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